SECTION 1 HARDWARE

SYSTEM OVERVIEW

Major system hardware components of the T100 Personal Computer are :

T100 System Unit	(PA7010)
Displays :	
Green Display	(PA7150)
Fine Color Display	(PA7161)
Liquid Crystal Display	(PA7170)
5-1/4" Floppy Disk Drive Unit	(PA7200)
Expansion Unit	(PA7300)
ROM/RAM Cartridges :	
RAM PACK 16	(PA7242)
RAM PACK 32	(PA7244)
Printers :	
Dot Matrix Printer P1010	(PA7251)
Dot Matrix Printer P1150	(PA7252)
Daisy Wheel Printer	(PA7254)

NOTE : Part numbers (PA mmmm) are suffixed by U, E, EB or EA depending on the AC power requirements.

The System Unit is the heart of your T100 system and consists of the CPU board, keyboard, power supply, speaker and cover.

The CPU board is placed horizontally in the base of the System Unit and includes the Z80A microprocessor, 32KB ROM, 64KB memory and peripheral interface with connectors. The ROM contains an enhanced version of the Microsoft BASIC-80 Interpreter.

The Keyboard is placed on the top of the System Unit and features 89 keys. The Keyboard has the typewriter and numeric pad layouts.

A base system requires one of three different displays – Green Display, Fine Color Display or Liquid Crystal Display.
The Green Display is a green phosphor display. The screen displays 25 lines of 80 characters or 24 lines of 36 characters. The screen can also display graphics in one of the resolutions, 160×100, 92×96, 640×200 or 288×192 picture elements.

The Fine Color Display can display characters and graphics in up to 8 colors. The screen has the same display capability as the Green Display.

The Liquid Crystal Display screen displays 8 lines of 40 characters and graphics in 320×64 picture elements. The Liquid Crystal Display provides a portable T100 configuration.

Since the System Unit allows the attachment of an audio cassette recorder for loading or saving information, the minimum T100 configuration is:

System Unit
One of the Displays
User-supplied audio cassette recorder

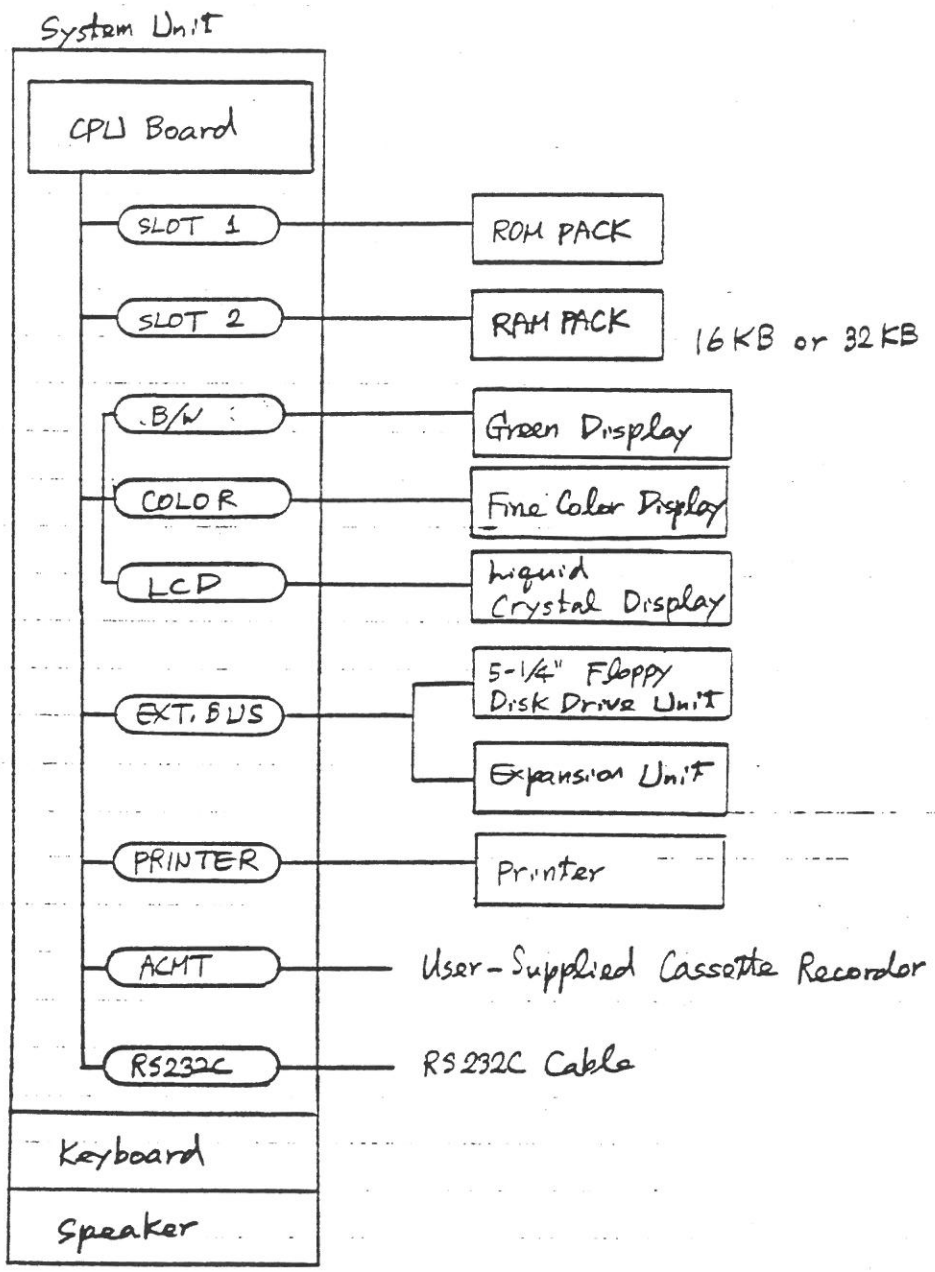
The 5-1/4" Floppy Disk Drive Unit has two 5-1/4" floppy disk drives. Each floppy disk inserted in the drive can store approximately 285KB of information.

The Expansion Unit permits the T100 system to have additional peripheral interfaces. The expansion boards can be inserted in five expansion slots

contained in the Expansion Unit.
Either a Floppy Disk Drive Unit or an Expansion Unit can be connected to the External Bus Connector on the back of the System Unit. If both units are required, the Expansion Unit is connected to the System Unit and the Floppy Disk Drive Unit is attached to a connector supplied on the back of the Expansion Unit.

The System Unit has two card edge sockets.
A battery-backup CMOS RAM PACK with 16KB or 32KB storage capacity can be plugged in one of the sockets. The RAM PACK can be used for loading and saving information. A ROM PACK can be plugged in the other socket. This adds another source for loading programs to the system.

The System Unit has a CENTRONICS printer port. One of three different printers can be attached to this port.



Notes: 1. ⬭ means connector.
2. 5-1/4" Floppy Disk Drive Unit can be connected through Expansion Unit.

Figure System Building Blocks

CPU BOARD

The CPU Board has dimensions of approximately 14.8 inches by 9.3 inches.

DC power from the power supply enter the board through a 4-pin connector.
2-pin speaker output connector and 25-pin keyboard connector are also attached on the CPU Board.

Other connectors on the board are :

- 44-pin card edge socket for ROM PACK
- 20-pin card edge socket for RAM PACK

These two sockets are accessed externally by opening the ROM/RAM PACK cover.

- RS232C port connector (25-pin D type)
- Printer connector (25-pin D type)
- External bus connector (50-pin D type)
- Green Display connector (phono jack)
- Liquid Crystal Display connector (8-pin DIN)
- Color Display connector (8-pin)
- Audio Cassette Recorder connector (8-pin DIN)

These connectors extend through the rear panel of the System Unit.

The RESET switch and the speaker volume control are also provided on the CPU Board and accessed on the back of the System Unit.

The major elements of the CPU Board are divided into six functional areas:

- The processor and its supporting elements
- Read-only memory (ROM)
- Random-access memory (RAM)
- I/O interface
- Display control
- External bus interface

The processor is the Z80A microprocessor which has 8-bit internal and bus structure. The processor is operated at 3.99 Mhz, which is derived by dividing a 15.9744 Mhz crystal by four.

Major supporting elements for the Z80A processor are Z80A PIO (parallel I/O) and Z80A CTC (timer/counters). These are used for keyboard control, speaker control, interrupt control and RAM refresh control.

The ROM consists of four 64K ROM modules providing 32KB of read-only memory. This contains the T-BASIC interpreter which is an enhanced version of the Microsoft BASIC-80 Interpreter without disk file functions. When an external ROM PACK is plugged in the System Unit, the external ROM precedes the integrated ROM.

The RAM consists of eight 64K dynamic RAM modules. This is standard and no expansion memory is offered for internal memory.

The I/O interface is supported by Z80A PIO, Z80A CTC (these are described above) and three Intel 8255 programmable peripheral interfaces. The i8255 PPIs are used for controlling display buffer, printer, audio cassette recorder, RS232C port and memory bank selection.

The display control is supported by the following components:

- i8255 PPIs
- CRT controller (HD46505S)
- Display buffer (Video RAM)
- Character generator

The display buffer consists of nine 16K RAM modules providing 16KB of memory (9 bits/byte).

The external bus interface is an extension of the Z80A microprocessor bus. This provides the 50-pin signal interface through the external bus connector.

CPU Board block diagram and component diagram are show on the following pages.

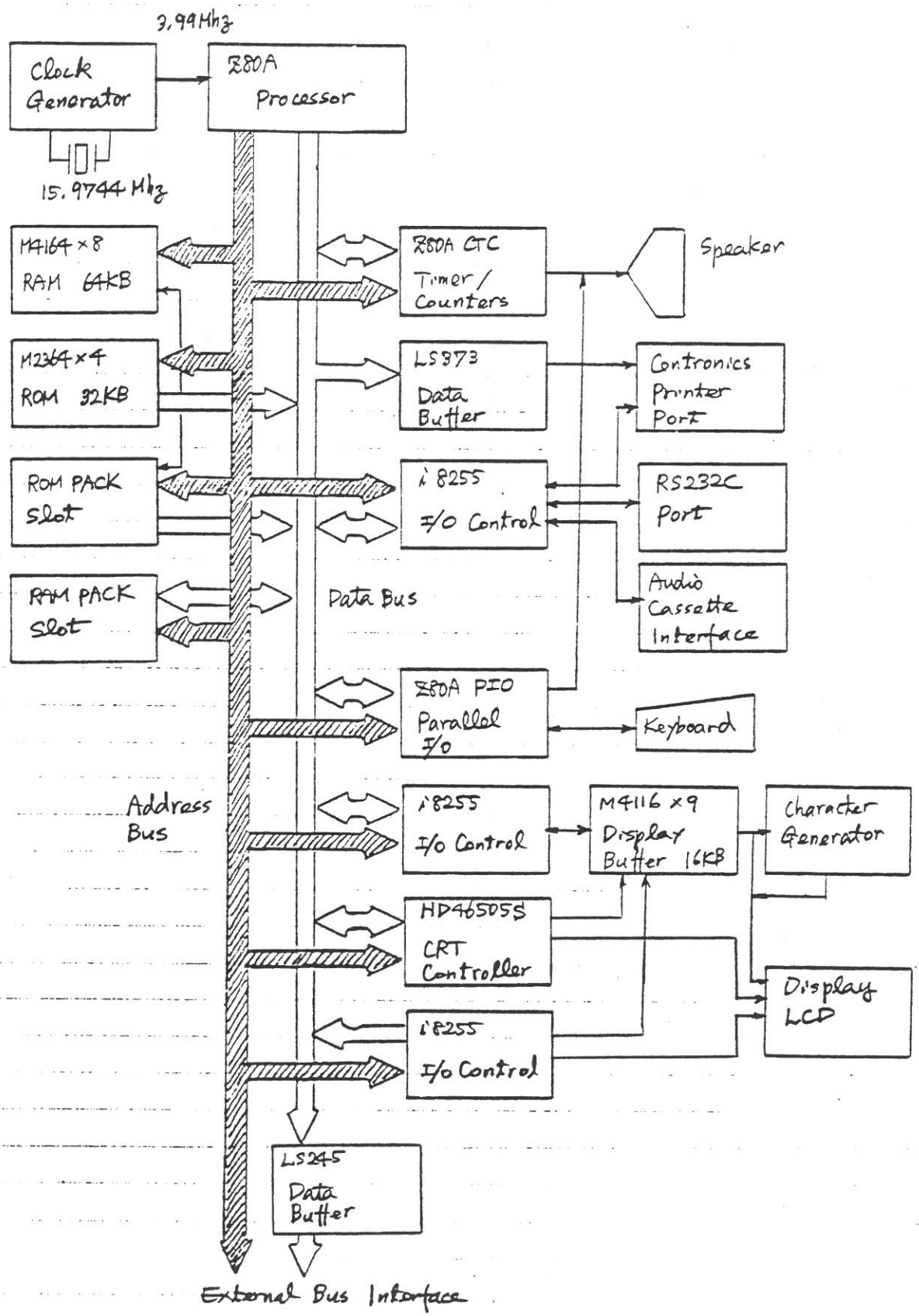


Figure CPU Board Block Diagram

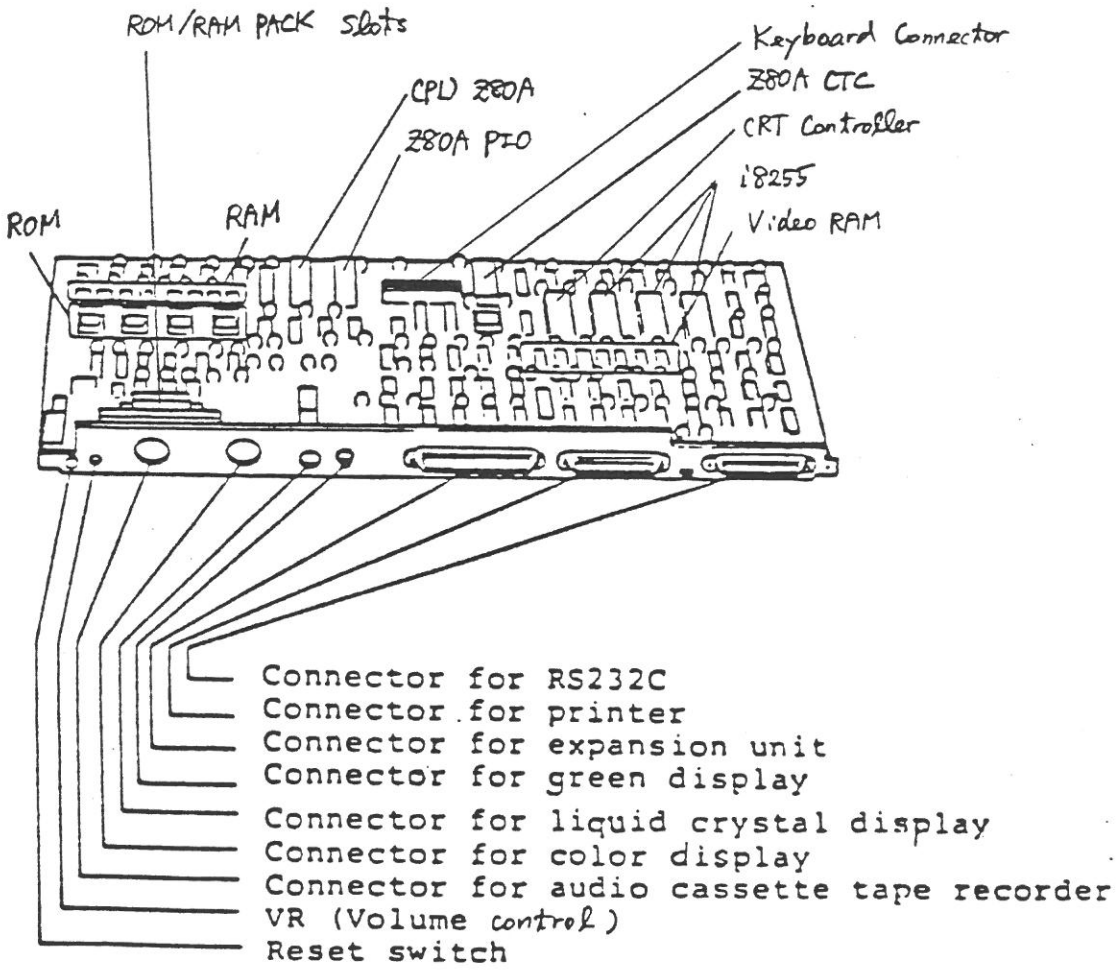


Figure CPU Board Component Diagram

MEMORY ADDRESS SPACE

The Z80A processor supports 16 bits of addressing (64KB of address space).
In T100, this address space can be configured from the following components:

- RAM 64KB
- Built-in ROM 32KB
- Optional ROM PACK (Max. 32KB)

When the RAM and the built-in ROM are used, the address space 0 through 32767 overlaps between RAM and ROM. Switching between these memories is performed by the memory bank selection.

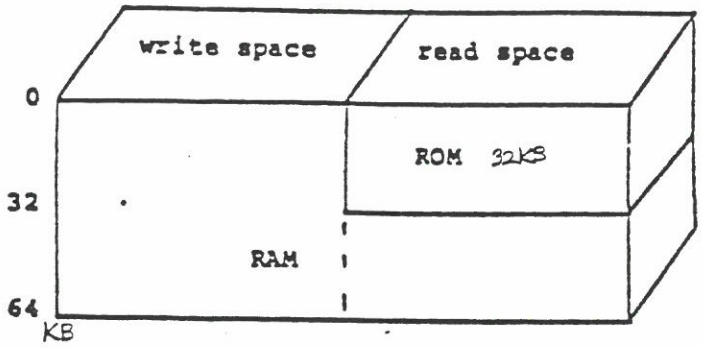
When your T100 has a Floppy Disk Drive unit, the software can be loaded from the disk to the RAM. T100 CP/M or T-DISK BASIC uses this method. The built-in ROM is used only for initial program loading from the disk and when the RAM is loaded with the software, only RAM configures 64KB address space.

If you plug a ROM PACK into the ROM PACK slot (Slot 1) of the System Unit, the program in the ROM PACK is executed at the system power-on and replaces the built-in ROM.

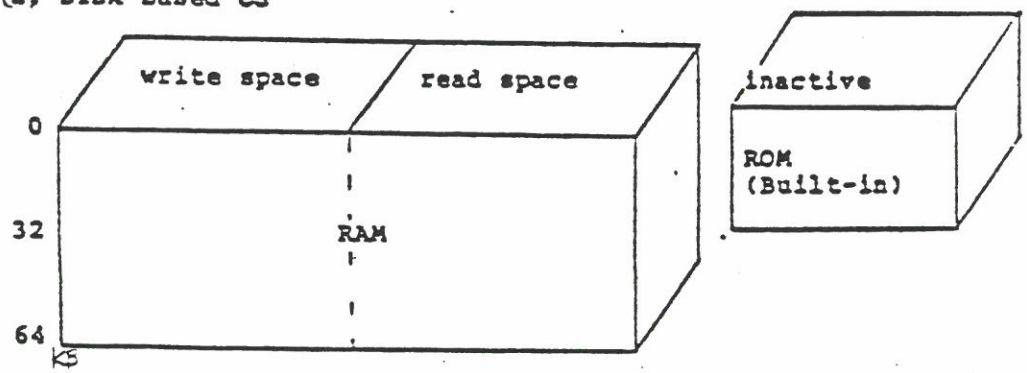
These memory address configurations are illustrated in the next page.

NOTE: The Video RAM (16KB) and optional RAM PACK (16KB or 32KB) are accessed through the I/O ports. These do not configure the main memory address space.

(1) Turn power on (Built-in T-BASIC)



(2) Disk based ~~es~~ software



(3) ROM ~~cartridge~~ PACK based

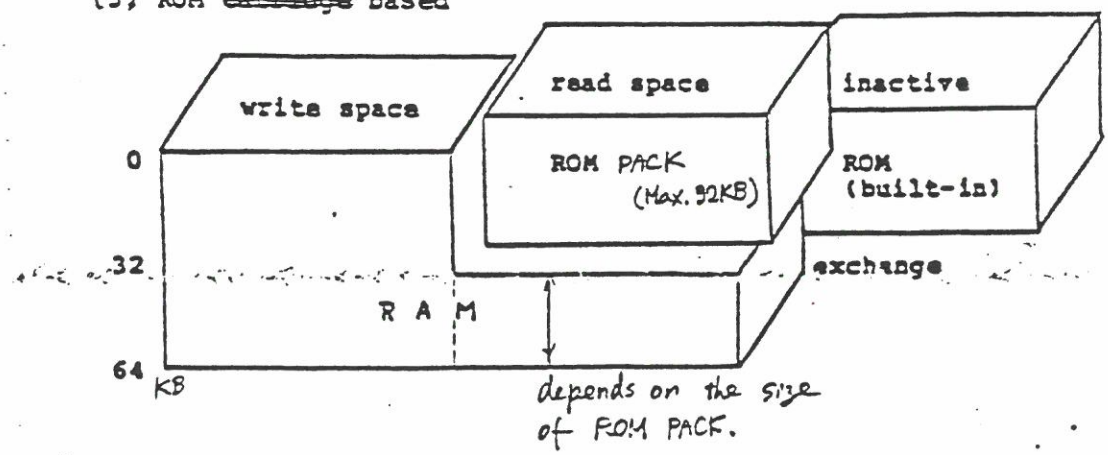


Figure Memory Configuration

▲ Memory Bank Selection ▲

Switching between the RAM and built-in ROM (or optional ROM PACK) can be made by the memory bank selection.

This is performed by executing the OUT instruction to the port 3C (hex). The format of a byte which is sent by the OUT instruction is as follows:

7	6	5	4	3	2	1	0
0	0	0	0	0	RST	RAM	ROM

Bit 7 through Bit 3 are not used.

Bit 2 (RST):
If this bit is 1, the hardware reset signal is generated, and the control is transferred to the address 0 of the memory specified by Bit 1 (RAM) or Bit 0 (ROM), after the OUT instruction has been executed.

Bit 1 (RAM):
If this bit is 1, the 64KB address space is configured only with RAM.
If this bit is 0, the 64KB address space is configured from RAM and either built-in ROM or ROM PACK, which is specified by Bit 0 (ROM).

Bit 0 (ROM):
This is effective only when Bit 1 is set to 0.
If this bit is 0, the built-in ROM is selected.
If this bit is 1, the ROM PACK is selected.

When the OUT instruction has been executed, the control is transferred as follows:

- If Bit 2 (RST) is 0, to the next instruction address of the memory specified by Bit 1 and Bit 0.
- If Bit 2 (RST) is 1, to address 0 of the memory specified by Bit 1 and Bit 0.

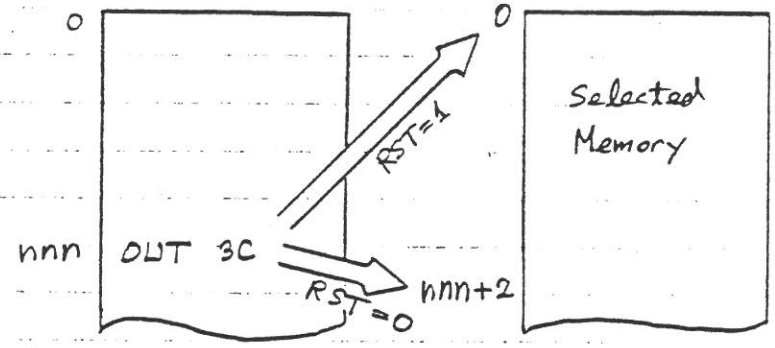


Figure Memory Bank Selection

The memory bank currently selected can be identified by reading a byte from the port 22 (hex). This byte is of the following format:

7	6	5	4	3	2	1	0
				ROM	RAM		

Bit 2 indicates the current bank:
1 : The current bank is RAM.
0 : The current bank is ROM.
Bit 1 indicates the type of ROM when Bit 2 is 0;
1 : ROM PACK 1
0 : Built-in ROM

When the current bank is ROM and a write operation is performed, the data is written to the identical address of the RAM. The address space for write operation is always RAM.

▲ I/O PORT ADDRESS MAP ▲

address	device	functions
00	8255PIO	CH.A DATA PORT (OUT ONLY) BIT 7-0 V-RAM ADDRESS 07-00
01	8255PIO	CH.B DATA PORT (OUT ONLY) BIT 7-0 V-RAM WRITE DATA
02	8255PIO	CH.C DATA PORT (INPUT ONLY) BIT 7-0 V-RAM READ DATA
03	8255PIO	CONTROL PORT
04-07	(Image)	
08	8255PIO	CH.A DATA PORT (OUT ONLY) BIT 7 HIGH-RESOLUTION MODE SET SIGNAL BIT 6 GRAPHIC MODE SET SIGNAL BIT 5 WIDE(80 COLUMN) CRT SET SIGNAL BIT 4-3 (NU) BIT 2-0 BACK COLOR SET SIGNAL (GREEN/RED/BLUE) LCD -- BIT 0 1:10 rasters 0: 8 rasters
09	8255PIO	CH.B DATA PORT (INPUT ONLY) BIT 7 ATTRIBUTE READ DATA BIT 6 CRT BUSY SIGNAL (HSYNC) BIT 5 V-SYNC SIGNAL BIT 4 DISPLAY TYPE (1:CRT, 0:LCD) BIT 3-0 (NU)
0A	8255PIO	CH.C DATA PORT (OUT ONLY) BIT 7 ATTRIBUTE WRITE DATA BIT 6 V-RAM READ SIGNAL (LOW-WRITE) BIT 5-0 V-RAM ADDRESS 13-08
0B	8255PIO	CONTROL PORT
0C-0F	(Image)	
10	HD46505S	REG. ADDRESS (OUT ONLY)
11	HD46505S	DATA PORT (OUT/IN) R00 H-TOTAL CHARCTER R01 H-DISPLAY CHARCTER R02 H-SYNC POSITION R03 SYNC PULSE WITH (VVVVHHHH) R04 V-TOTAL CHARCTER R05 TOTAL RASTER ADJUST R06 V-DISPLAY CHARCTER R07 V-SYNC POSITION R08 INTERLACE AND SCEW (CCDD--VS) R09 MAX. RASTER ADDRESS R10 CURSOR START RASTER (-BPDDDDD)

I/o Address Map (continued)

address	device	functions
		R11 CURSOR STOP RASTER R12 START ADDRESS HIGH R13 START ADDRESS LOW R14 CURSOR ADDRESS HIGH R15 CURSOR ADDRESS LOW
12-17	(Image)	
18		ROM/RAM PACKAGE PORT #0
19		ROM/RAM PACKAGE PORT #1
1A		ROM/RAM PACKAGE PORT #2
1B		ROM/RAM PACKAGE PORT #3
1C-1F	(RFU)	
20	8255PIO	CH.A DATA PORT (OUT ONLY) BIT 7 PRINTER PRIME SIGNAL BIT 6 ← PRINTER STROBE SIGNAL BIT 5 ACMT REMOTE CONTROL SIGNAL (LOW) BIT 4 ACMT WRITE DATA BIT 3-0 (NU)
21	8255PIO	CH.B DATA PORT (INPUT ONLY) BIT 7 PRINTER FAULT SIGNAL (LOW) BIT 6 PRINTER BUSY SIGNAL BIT 5 ACMT READ-OUT DATA BIT 4 SIO CI/TXC (LOW) BIT 3 DCD (LOW) BIT 2 DSR (LOW) BIT 1 CTS (LOW) BIT 0 RXD
22	8255PIO	CH.C DATA PORT (GA=OUT, GB=IN) BIT 7 SIO ST1 (LOW-OUT) BIT 6 DTR (LOW-OUT) BIT 5 RTS (LOW-OUT) BIT 4 TXD (OUT) BIT 3-2 MEMORY MODE 10: CASSETTE 01: PAM 00: INT.ROM ROM PACK BIT 1-0 (NU.IN) CONTROL PORT
23	8255PIO	
24-27	(Image)	

I/o Address Map (continued)

address	device	
28	Z80A-CTC	CH.0 ACMT/RS232C TIMING CNT.
29	Z80A-CTC	CH.1 SPEAKER FREQUENCY
2A	Z80A-CTC	CH.2 KB TIMING CONTROL
2B	Z80A-CTC	CH.3 SYSTEM CLOCK DDDDDDD1 CONTROL WORD BIT 7 INT. ENABLE ON 1 BIT 6 MODE TIMER (0)/COUNTER (1) BIT 5 PRESCALER 256(1)/16(0) BIT 4 EDGE SELECT FALLING(0)/RISING(1) BIT 3 TIMER TRIGGER 0:AUTOMATIC TRIGGER WHEN TIME CONSTANT IS LOADED 1:CLK/TRG PULSE STARTS TIMER BIT 2 TIME CONSTANT FOLLOWS ON 1 BIT 1 SOFTWARE RESET DDDDDXX0 INTERRUPT VECTOR WORD
2C-2F	(Image)	
30	Z80A-PIO	CH.A DATA PORT (OUT ONLY) BIT 7 ALARM ON FOR SPEAKER BIT 6-4 KB SCAN-BLOCK SELECT BIT 3-0 KB SCAN-LINE SELECT
31	Z80A-PIO	CH.B DATA PORT (INPUT ONLY) BIT 7-0 KB SCAN-INPUT DATA (LOW LEVEL)
32	Z80A-PIO	CH.A CONTROL PORT DD--1111 MODE CONTROL WORD 00 MODE-0 BYTE INPUT 01 1 OUTPUT 10 2 BIDIRECTIONAL 11 3 BIT INPUT/OUTPUT DDDDDDD0 INTERRUPT VECTOR WORD DDDDDDDD IN/OUT CONTROL AND MASK CONTROL DDDD0111 INTERRUPT CONTROL WORD BIT 7 INT.ENABLE(1)/DISABLE(0) BIT 6 AND(1)/OR(0) FUNCTION BIT 5 ACTIVE LEVEL HIGH(1)/LOW(0) BIT 4 MASK WORD FOLLOWS ON 1
33	Z80A-PIO	CH.B CONTROL PORT
34-37	(Image)	

I/o Address Map (continued)

address	device	functions
38		LATCH FOR PRINT OUT DATA
39-3B	(Image)	
3C		MEMORY MODE SELECT AND RESET BIT 7-3 (NU) BIT 2H/W RESET BIT 1RAM SELECT BIT 0ROM SELECT (1:pac,0:int)
3D-3F	(Image)	
40-4F	(RPU)	
50-DF	FOR EXPANSION UNIT	
E0		FDC TC SIGNAL OFF
E1	(Image)	
E2		FDC TC SIGNAL ON
E3	(Image)	
E4	uPD765	STATUS REGISTER (INPUT ONLY) BIT 7REQUEST FOR MASTER BIT 6DATA INPUT (0)/OUTPUT (1) BIT 5NON DMA MODE BIT 4FDC BUSY BIT 3-0 FDD#3-#0 BUSY
E5	uPD765	DATA(REGISTER) READ/WRITE PORT
E6	uPD765	FDC CONTROL PORT BIT 7RESET(1) SIGNAL OUTPUT. INT SIGNAL INPUT BIT 6MOTOR ON(1) SIGNAL OUTPUT BIT 5-4 PRE-SHIFT 1/0 CONTROL(Don't use=00) BIT 3-0 (NU)
E7-EF	(Image)	
F0-FF	(RFU)	

▲ KEYBOARD AND SPEAKER INTERFACE ▲

The keyboard is controlled by the Z80A PIO. The PIO performs the following functions:

- Enable / disable keyboard scanning
- Select scan lines
- Obtain scan codes

Reflected scan codes are transformed to ASCII codes by the keyboard I/O driver.

In addition to the keyboard control, the Z80A PIO uses one output bit to enable / disable the speaker. The speaker is drived by the Z80A CTC.

▲ Keyboard Control ▲

A block diagram of the keyboard / speaker interface, and table of keyboard scan signals are on the following pages.

The keyboard scan lines are divided into three groups (scan blocks A, B and C). Each block is enabled by setting the corresponding bit of A4, A5 and A6 of the port A of PIO.

Each block has four scan lines to keyboard. Each scan line is activated by setting the corresponding bit of A0 through A3 of the port A of PIO.

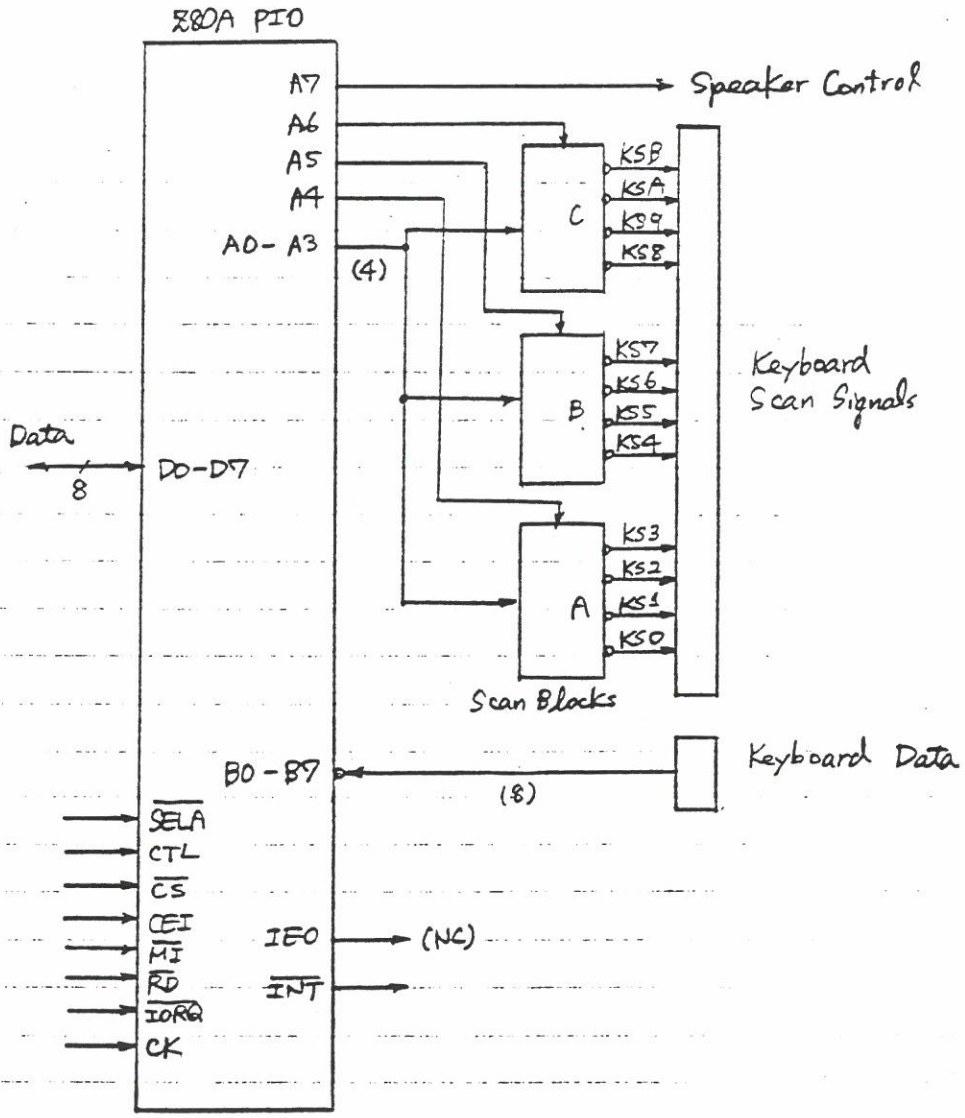


Figure ____ Keyboard / Speaker Interface Block Diagram

Port	Pin	Active	Function
A (30H)	A7	High	Enables speaker.
	A6	High	Enables scan block C.
	A5	High	Enables scan block B.
	A4	High	Enables scan block A.
	A3	High	Selects scan line in each block.
	A2	High	
	A1	High	
	A0	High	
B (31H)	B7	Low	Reflects the key pressed.
	B6	Low	
	B5	Low	
	B4	Low	
	B3	Low	
	B2	Low	
	B1	Low	
	B0	Low	

Table ___ PIO Keyboard Scan Signals

The keyboard scan is performed as follows:

- Enable all scan lines.
- Accept interrupt from port B of PIO. This occurs when one of the keys are pressed, thereby the corresponding line of port B is set to low level.
- Scan the lines selectively and get the scan code from port B. This identifies the key which has been pressed.

This cycle is activated every 16ms by the Z80A CTC interrupt (channel 2).

A table of keyboard scan codes is on the following page.

Each scan code is converted to the corresponding ASCII code by the keyboard I/O driver. SHIFT, CTRL, GRAPH and CAPS LOCK keys are defined as shift keys in translation.

Up to 20 codes are buffered in the keyboard ring buffer. This is performed regardless of the system requesting the keyboard input.

All data keys are defined as typematic. A key which is held down is scanned every 50 ms.

Examples of T-BASIC programs for clearing the keyboard ring buffer and keyboard scan are shown on the following pages.

Scan Block	Scan Line	Scan Signal	Scan Codes (Low Level)							
A6 A5 A4	A3 A2 A1 A0		B7	B6	B5	B4	B3	B2	B1	B0
Block A 001	0 0 0 1	KS0								
	0 0 1 0	KS1								
	0 1 0 0	KS2								
	1 0 0 0	KS3								
Block B 010	0 0 0 1	KS4								
	0 0 1 0	KS5								
	0 1 0 0	KS6								
	1 0 0 0	KS7								
Block C 100	0 0 0 1	KS8								
	0 0 1 0	KS9								
	0 1 0 0	KSA								
	1 0 0 0	KSB								

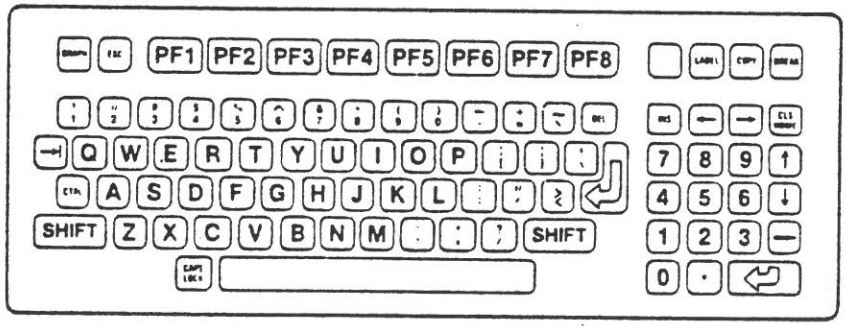


Figure Keyboard Scan Codes

```
10 FOR Z=1 TO 20:GOSUB 70:NEXT
20 FOR I=&HFF01 TO &HFF20:POKE I,0:NEXT
30 PRINT
40 INPUT A$
50 PRINT A$
60 END
70 PRINT:FOR I=&HFF01 TO &HFF20:PRINT CHR$(PEEK(I));" ";:NEXT:RETURN
```

```
? abcde
abcde
OK
```

Figure A Program for Clearing Keyboard Buffer

```
10 '*** KEY SCAN ***      T-DISK BASIC
100 SCAN$=STRING$(25,0):KBL$="  ":KBD$="  "
110 SCN=VARPTR(SCAN$)+1:IF SCN<0 THEN SCN=SCN+65536!
120 SCAN=PEEK(SCN)+PEEK(SCN+1)*256
130 KB1=VARPTR(KBL$)+1:IF KB1<0 THEN KB1=KB1+65536!
140 KBA=PEEK(KB1)+PEEK(KB1+1)*256
150 KB2=VARPTR(KBD$)+1:IF KB2<0 THEN KB2=KB2+65536!
160 KBB=PEEK(KB2)+PEEK(KB2+1)*256
170 POKE SCAN,&HF5:'      PUSH    PSW
180 POKE SCAN+1,&H3A:'    LDA     KBA       ;get scan line data
190 POKE SCAN+2,KBA-INT(KBA/256)*256
200 POKE SCAN+3,INT(KBA/256)
210 POKE SCAN+4,&HF3:'    DI                ;disable interrupt
220 POKE SCAN+5,&HD3:'    OUT     30H       ;output scan data
230 POKE SCAN+6,&H30
240 POKE SCAN+7,&HFB:'    EI                ;enable interrupt
250 POKE SCAN+8,&HDB:'    IN      31H       ;input data read
260 POKE SCAN+9,&H31
270 POKE SCAN+10,&HEE:'   XRI     0FFH      ;bit level change
280 POKE SCAN+11,&HFF
290 POKE SCAN+12,&H32:'   STA     KBB       ;read data set to KBB$
300 POKE SCAN+13,KBB-INT(KBB/256)*256
310 POKE SCAN+14,INT(KBB/256)
320 POKE SCAN+15,&H3E:'   MVI     A,7FH
330 POKE SCAN+16,&H7F
340 POKE SCAN+17,&HD3:'   OUT     30H       ;scan line restore
350 POKE SCAN+18,&H30
360 POKE SCAN+19,&HF1:'   POP     PSW
370 POKE SCAN+20,&HC9:'   RET               ;return
1000 WIDTH 80:OVER=TIME:CLS:COLOR 7,1
1010 X%=40:XX%=X%:Y%=12:YY%=Y%
1020 KBD$="  "
1030 LOCATE X%,Y%:PRINT "■";
1040 POKE KBA,&H12
1050 IF TIME-OVER=120 THEN GOTO 1000
1060 CALL SCAN:' SCAN LINE=1
1070 IF PEEK(KBB)=&H4 THEN YY%=Y%+1:GOTO 2000
1080 IF PEEK(KBB)=&H10 THEN XX%=X%-1:GOTO 2000
1090 IF PEEK(KBB)=&H40 THEN XX%=X%+1:GOTO 2000
1100 POKE KBA,&H14:CALL SCAN:' SCAN LINE=2
1110 IF PEEK(KBB)=&H1 THEN YY%=Y%-1:GOTO 2000
1120 GOTO 1040
2000 LOCATE X%,Y%:PRINT "・";
2010 IF XX%<0 THEN GOTO 2040
2020 IF XX%>78 THEN GOTO 2040
2030 X%=XX%
2040 IF YY%<0 THEN GOTO 1030
2050 IF YY%>24 THEN GOTO 1030
2060 Y%=YY%:GOTO 1030
```

Figure A Keyboard Scan Program

◢ Speaker Control ◣

The speaker is drived by the Z80A PIO and Z80A CTC as follows:

Port	Device	Bits	Functions
30H	PIO Channel A	Bit 7	1 -- Enable speaker
			0 -- Disable speaker
29H	CTC Channel 1		Speaker Frequency
2BH	CTC Channel 3	Bit 5	Prescaler
			1 -- 1/256
			0 -- 1/16

Output "1" to bit 7 of PIO channel A enables the speaker. Contents of a byte output to the CTC channel 1 specifies a speaker frequency. When this byte is output to the CTC channel 1, the speaker continues to sound. This is terminated by sending "0" to bit 7 of PIO channel A.

The speaker frequency is scaled by the CTC channel 3, Bit 5. Sending "1" sets the speaker to low frequency. Sending "0" sets the speaker to high frequency.

T-BASIC interpreter uses a table for selecting the speaker frequency. This table is shown on the following page.

Para	Freq.	Para	Freq.
0(239)	33Hz	1(225)	35Hz
2(213)	37Hz	3(201)	39Hz
4(190)	41Hz	5(179)	44Hz
6(169)	46Hz	7(159)	49Hz
8(150)	52Hz	9(142)	55Hz
10(134)	58Hz	11(127)	62Hz
12(119)	66Hz	13(113)	69Hz
14(106)	74Hz	15(100)	78Hz
16(95)	82Hz	17(89)	88Hz
18(84)	93Hz	19(80)	98Hz
20(75)	104Hz	21(71)	110Hz
22(67)	117Hz	23(63)	124Hz
24(60)	130Hz	25(56)	140Hz
26(53)	147Hz	27(50)	156Hz
28(47)	166Hz	29(45)	174Hz
30(42)	186Hz	31(40)	195Hz
32(38)	206Hz	33(36)	217Hz
34(34)	230Hz	35(32)	244Hz
36(30)	260Hz	37(28)	279Hz
38(27)	289Hz	39(25)	313Hz
40(24)	326Hz	41(22)	355Hz
42(21)	372Hz	43(20)	391Hz
44(19)	411Hz	45(18)	434Hz
46(17)	460Hz	47(253)	494Hz
48(239)	523Hz	49(225)	556Hz
50(213)	587Hz	51(201)	622Hz
52(190)	658Hz	53(179)	698Hz
54(169)	740Hz	55(159)	786Hz
56(150)	833Hz	57(142)	880Hz
58(134)	933Hz	59(127)	984Hz
60(119)	1050Hz	61(113)	1106Hz
62(106)	1179Hz	63(100)	1250Hz
64(95)	1316Hz	65(89)	1404Hz
66(84)	1488Hz	67(80)	1563Hz
68(75)	1667Hz	69(71)	1761Hz
70(67)	1866Hz	71(63)	1984Hz
72(60)	2083Hz	73(56)	2232Hz
74(53)	2358Hz	75(50)	2500Hz
76(47)	2660Hz	77(45)	2778Hz
78(42)	2976Hz	79(40)	3125Hz
80(38)	3289Hz	81(36)	3472Hz
82(34)	3676Hz		

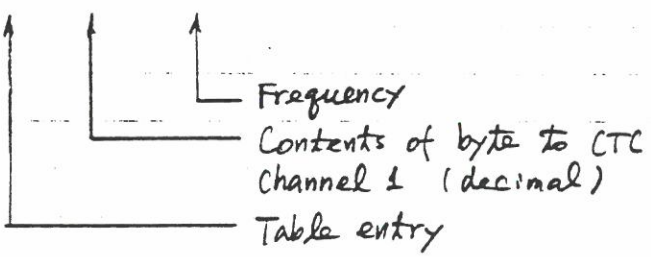


Table T-BASIC Speaker Frequency Table

DISPLAY INTERFACE

The T200 display interface is designed to attach Green Display, Fine Color Display, Liquid Crystal Display or TV set (user-supplied RF modulator is required for TV set). The connectors provided are:

- Composite phono jack for Green Display
- 8-pin DIN connector for Fine Color Display or for an RF modulator
- 8-pin connector for Liquid Crystal Display

The interface is capable of operating in the 80x25 character or 36x24 character mode, TEXT, GRAPHICS or HIGH RES (high-resolution graphics) mode, and monochrome or color mode.

The screen modes are summarized in the following table:

Display	Modes	Picture Elements	Colored Picture Elements	Chars. x Line
CRT	TEXT			80 x 25 36 x 24
	GRAPHICS	160 x 100 72 x 96	160 x 100 72 x 96	80 x 25 36 x 24
	HIGH RES	640 x 200 288 x 192	80 x 200 36 x 192	80 x 25 36 x 24
LCD	TEXT HIGH RES	 320 x 64		40 x 8 40 x 8

Table Screen Modes

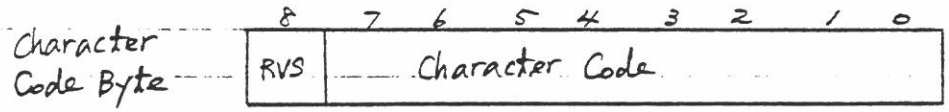
♪ Screen Modes ♪

TEXT Mode

In TEXT mode, the display can be operated in 36×24 character mode for low-resolution monitors or TV sets, in 80×25 character mode for high-resolution monitors, or in 40×8 (or 6) character mode for Liquid Crystal Display.

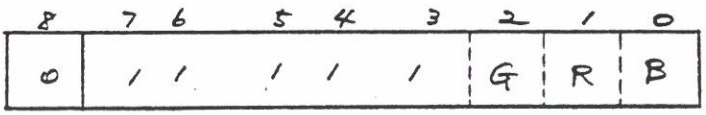
Characters are formed by 8×8 dot patterns from the Character Generator. The Character Generator (ROM) contains dot patterns for 192 characters.

Every display character position is defined by a Character Code Byte stored in the display buffer. This has the following format:



When the bit 8 of a Character Code Byte is set to "1", the character is displayed in reverse video in monochrome mode or displayed by exchanging the foreground / background colors in color mode. Reverse video display is effective on 8×8 dot matrix.

The display buffer can also contain Color Attribute Bytes. This has the following format:



When a byte in the display buffer has "0" in bit 8 and "1" in bit 7 through 3, this byte is identified as a Color Attribute Byte. This specifies the foreground color of characters displayed until another Color Attribute Byte appears. A space character is output by the Character Generator when a Color Attribute Byte is found in the display buffer. Consequently a space character is displayed on the corresponding position of the screen.

The foreground colors are defined as follows:

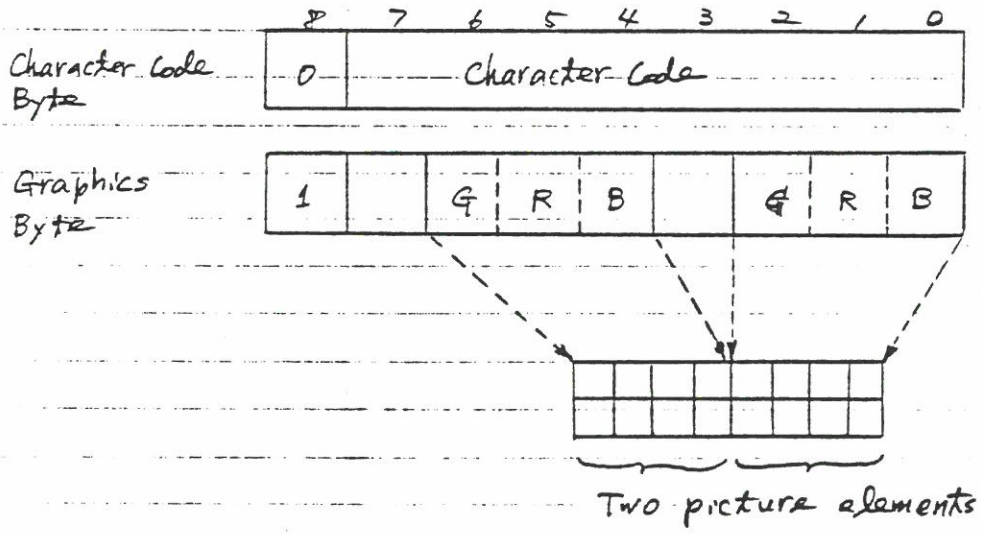
G R B	Color
0 0 0	Black
0 0 1	Blue
0 1 0	Red
0 1 1	Magenda
1 0 0	Green
1 0 1	Cyan
1 1 0	Yellow
1 1 1	White

These bits give the level of intensity for monochrome mode. The background color of a screen is defined by output of 8255 PPI. This is explained later in this chapter. For Liquid Crystal Display, bits 2 through 0 of the Color Attribute Byte have different meanings. This is also described later.

GRAPHICS Mode

In GRAPHIC mode, each picture element is defined as 4×2 raster units on the display screen. The graphics resolution is 160×100 for 80×25 character mode or 72×96 for 36×24 character mode.

A horizontal combination of two picture elements is defined by one byte in the display buffer. This corresponds to the Attribute Byte in the TEXT mode. Character Code Bytes in the TEXT mode can be used to display characters in the GRAPHICS mode. Those two bytes have the following format in the display buffer:



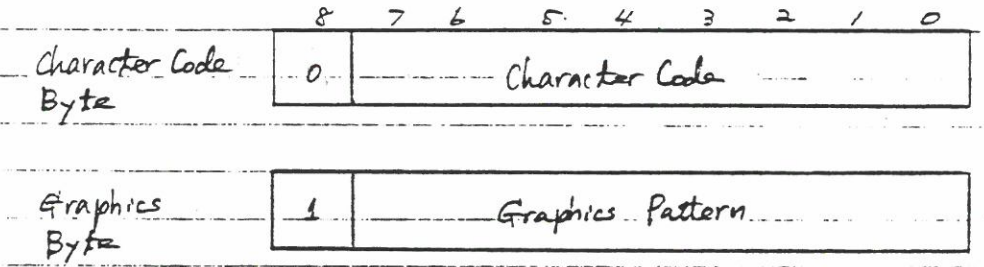
Bits 6 through 4 of the Graphics Byte specifies the color of left picture element and bits 2 through 0 of the Graphics Byte specifies the color of right picture element for each horizontal combination of picture elements.

When a byte in the display buffer has "1" in bit 8, this byte is identified as a Graphics Byte. Consequently, the reverse video bit (bit 8) of the Character Code Byte cannot be used in the GRAPHICS mode.

HIGH RES Mode

In HIGH RES mode, each picture element is defined as one raster unit on the display screen. The graphics resolution is 640 x 200 for 80 x 25 character mode or 288 x 192 for 36 x 24 character mode.

An 8-bit pattern is stored in each HIGH RES Graphics Byte in the display buffer. Character Code Bytes can be used to display characters.



Bit 8 of each byte in the display buffer is used to identify the Graphics Byte. Consequently, the reverse video bit (bit 8) of the Character Code Byte cannot be used.

In HIGH RES mode, graphics cannot be colored on per picture element basis. The Attribute Byte as defined in the TEXT mode can be used to color the graphics. When this byte is used, the graphics are colored as follows:

- 8 x 8 picture elements (as in character pattern) are colored by the color specified in an Attribute Byte.
- Subsequent 8 x 8 picture elements are colored by the same color until another Attribute Byte appears.

- The 8×8 picture elements which corresponds to the Attribute Byte position are replaced by a space character.

Display Control

The display interface is composed of the following major elements:

- Two 8255 PPIs (8255-1, 8255-2)
- CRT Controller (HD46505S)
- Display Buffer (Video RAM)

8255 PPIs

The 8255 PPIs identify the type of display unit attached and perform read/write operations for Video RAM, selection of screen modes, and selection of background color.

A block diagram of 8255 display interface and a table of control functions are on the following pages.

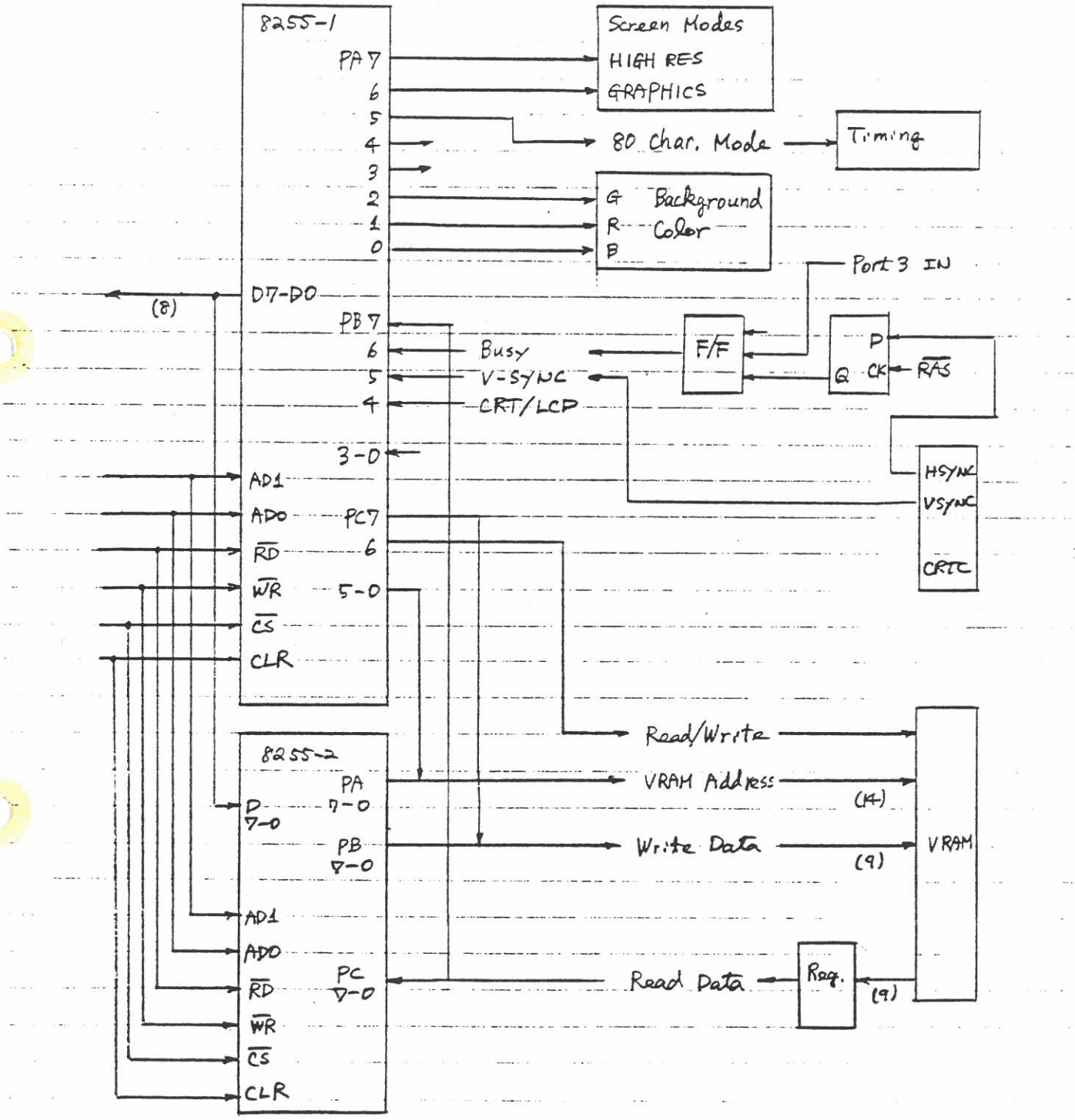


Figure 8255 Display Interface Block Diagram

	Port	Pin	Active	Functions
	A (08H) Output	PA7	H	Selects HIGH RES mode.
		6	H	Selects GRAPHICS mode.
		5	H	Selects 80-char. mode.
		4	—	
		3	—	
		2	H	G } Specifies a background
		1	H	R } color for CRT.
		0	H	B }
8255-1	B (09H) Input	PB7	H	Reads data (2^8) from VRAM.
		6	H	Reads VRAM busy signal.
		5	H	Reads V-SYNC signal.
		4	H	Identifies the type of display (1 = CRT, 0 = LCD).
		3-0		
	C (0AH) Output	PC7	H	Writes data (2^8) to VRAM.
		6	L	Sets VRAM R/W mode (1 = Read, 0 = Write).
		5-0	H	Sends VRAM address ($2^{13} - 2^8$)
8255-2	A (00H) Output	PA 7-0	H	Sends VRAM address ($2^7 - 2^0$)
	B (01H) Output	PB 7-0	H	Writes data ($2^7 - 2^0$) to VRAM.
	C (02H) Input	PC 7-0	H	Reads data ($2^7 - 2^0$) from VRAM

Notes are on the following page.

Table 8255 Display Control Functions

NOTES:

- If both PA7 and PA6 for screen modes are set to "1", the screen mode becomes HIGH RES mode.

- When PA6 is set to "1", the screen is in 80 x 25 character mode and 14Mhz video bandwidth is used.
  When PA6 is set to "0", the screen is in 36 x 24 character mode and 7Mhz video bandwidth is used.
  The CRT Controller parameters must be set accordingly.
  The Liquid Crystal Display is not affected by this signal.

- PA2 through PA0 specify a background color for CRT display. These function differently for LCD. This is described later in this chapter.

CRT Controller

The CRT Controller (HD46505S) povides the interface to drive a CRT display or Liquid Crystal Display. The following tables summarize the HD46505S internal data registers and their functions and parameters.

Addr. Reg.	Reg. #	Register Type	Program Unit	I/O	Data Bits 7 6 5 4 3 2 1 0
—	AR	Address Register	—	W	x x x
0	R0	Horizontal Total	Char.	W	
1	R1	Horizontal Displayed	Char.	W	
2	R2	Horiz. Sync Position	Char.	W	
3	R3	Sync Pulse Value	Char./Rast.	W	V V V V H H H H
4	R4	Vertical Total	Line	W	x
5	R5	Total Raster Adjust	Raster	W	x x x
6	R6	Vertical Displayed	Line	W	x
7	R7	Vert. Sync Position	Line	W	x
8	R8	Interlace and Skew	—	W	c c d d x x V S
9	R9	Max Raster Address	Raster	W	x x x
A	R10	Cursor Start	Raster	W	x B P
B	R11	Cursor End	Raster	W	x x x
C	R12	Start Addr. (H)		R/W	x x
D	R13	Start Addr. (L)		R/W	
E	R14	Cursor Addr. (H)		R/W	x x
F	R15	Cursor Addr. (L)		R/W	
10	R16	Light Pen (H)		R	x x
11	R17	Light Pen (L)		R	

Table CRT Register Description

Addr. Reg.	Reg. #	Register Type	CRT		LCD	
			36 x 24	80 x 25	40 x 8	40 x 6
	AR	Address Register				
0	R0	Horizontal Total	57-1	114-1	95-1	95-1
1	R1	Horizontal Displayed	37	81	82	82
2	R2	Horiz. Sync Position	47-1	94-1	85	85
3	R3	Sync Pulse Value	34H	33H	16H	16H
4	R4	Vertical Total	32-1	32-1	4-1	3-1
5	R5	Total Raster Adjust	6	6	0	2
6	R6	Vertical Displayed	24	25	4	3
7	R7	Vert. Sync Position	29-1	29-1	0	0
8	R8	Interlace and Skew	50H	50H	50H	50H
9	R9	Max Raster Address	7	7	7	9
A	R10	Cursor Start	47H	47H	47H	47H
B	R11	Cursor End	07H	07H	07H	07H
C	R12	Start Addr. (H)				
D	R13	Start Addr. (L)				
E	R14	Cursor Addr. (H)				
F	R15	Cursor Addr. (L)				
10	R16	Light Pen (H)				
11	R17	Light Pen (L)				

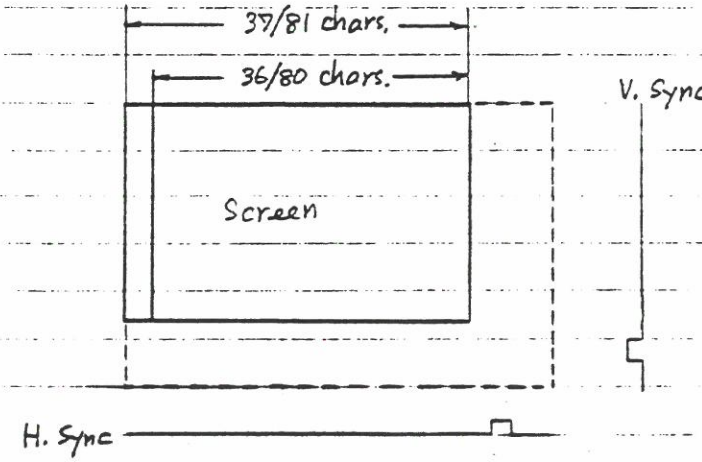
Table ___ CRT Controller Register Values

The alternative values for Registers R0 through R9 are defined in the CRT I/O driver and values pertinent to the display attached are loaded to the Registers.

The contents of R10 (Cursor Start) are changed to 45H when the CAPS LOCK key has been pressed:

CAPS LOCK	(R10)	Cursor Shape
NO	47H	
YES	45H	

Screen size in characters (R0, R4) and synchronization signals (R2, R7) are defined as shown in the following figure:



Each line is preceded by a Color Attribute Byte, which sets the default color and is not displayed on the screen.

The access to the Video RAM by the processor is allowed only during the horizontal synchronization time. Procedures to access the Video RAM is shown on the following page.

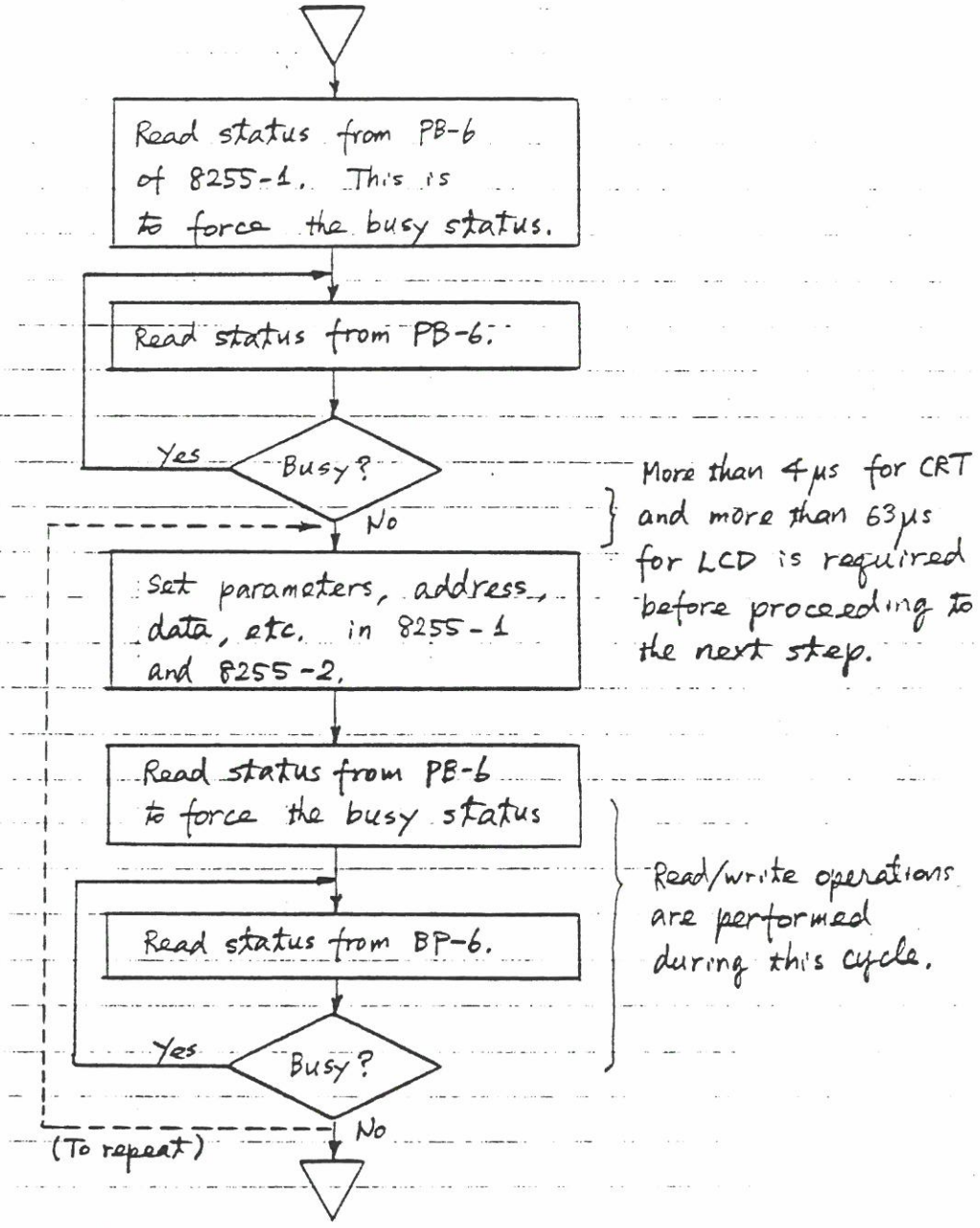


Figure Access to Video RAM

An example of Video RAM access program is on the following pages.

```
10 '*** V-RAM READ WRITE SAMPLE ***  T-BASIC
20 DIM A1(2),A2(2),A3(2)
30 SUB1$=STRING$(44,44):SUB2$=STRING$(50,50)
40 RESTORE
50 VRW=VARPTR(SUB1$)+1:IF VRW<0 THEN VRW=VRW+65536!
60 VRWR=PEEK(VRW)+PEEK(VRW+1)*256:'   V-RAM write routine
70 VRR=VARPTR(SUB2$)+1:IF VRR<0 THEN VRR=VRR+65536!
80 VRRD=PEEK(VRR)+PEEK(VRR+1)*256:'   V-RAM read routine
90 MADR=VRWR:GOSUB 1000:'             set write routine
100 MADR=VRRD:GOSUB 1000:'            set read routine
110 VRRDA=VRRD+47:VRRDB=VRRD+48
120 POKE VRRD+38,VRRDA-INT(VRRDA/256)*256
130 POKE VRRD+39,INT(VRRDA/256)
140 POKE VRRD+43,VRRDB-INT(VRRDB/256)*256
150 POKE VRRD+44,INT(VRRDB/256)
200 '
210 ' ** test data display **
220 RESTORE 3020:WIDTH 36:SCREEN 1:CLS:' graphic display mode
230 READ X1:IF X1<0 THEN 260
240 READ Y1,X2,Y2,C:'    read parameter
250 LINE(X1,Y1)-(X2,Y2),C:GOTO 230
260 READ X1:IF X1<0 THEN 300
270 READ Y1,C:'          read parameter
280 PSET(X1,Y1),C:GOTO 260
300 '
310 ' copy test data
320 '
330 OUT &H10,12:STA=INP(&H11)*256
340 OUT &H10,13:STA=STA+INP(&H11)+1:' V-RAM start address
345 IF STA>2047 THEN STA=STA-2048:GOTO 345:' start address masking 2KB
350 '
360 FOR ROW=2 TO 4
370 A1(1)=STA+ROW*37+4
380  FOR CPY=1 TO 3
390  A1(2)=STA+(ROW+CPY*4)*37+4+CPY*3
400   FOR BLK=0 TO 12288 STEP 4096
410    FOR CLM=0 TO 21
420     FOR I=1 TO 2
430     A2(I)=A1(I)+CLM
440     IF A2(1)>2047 THEN A2(I)=A2(I)-2048
450     A3(I)=A2(I)+BLK
460     NEXT I
470    POKE VRRD+16,A3(1)-INT(A3(1)/256)*256:' V-RAM address
480    POKE VRRD+20,INT(A3(1)/256)
490    CALL VRRD:'                    read test data
500    OUT &H1,PEEK(VRRDB):'          read data to write data
510    POKE VRWR+16,A3(2)-INT(A3(2)/256)*256:' V-RAM address
520    POKE VRWR+20,INT(A3(2)/256)+PEEK(VRRDA)
530    CALL VRWR:'                    write copy data
540    NEXT CLM
550   NEXT BLK
560  NEXT CPY
570 NEXT ROW
580 GOTO 220
```

資料番号

```
1000 '
1010 ' assembler command set
1020 READ D:'          command read
1030 IF D=255 THEN RETURN
1040 POKE MADR,D:'   command set to memory
1050 MADR=MADR+1:GOTO 1020
2000 '
2010 ' *** write routine ***
2020 DATA 243:'        DI                ;disable interrupt
2030 DATA 219,9:'      IN     09H        ;dummy read
2040 DATA 219,9:'      IN     09H        ;status read
2050 DATA 230,64:'     ANI    40H
2060 DATA 32,250:'     JR     NZ,*-4     ;wait H-SYNC ON
2070 DATA 219,9:'      IN     09H        ;status read
2080 DATA 230,64:'     ANI    40H
2090 DATA 40,250:'     JR     Z,*-4      ;wait H-SYNC OFF
2100 DATA 62,0:'       MVI    A,00H
2110 DATA 211,0:'      OUT    00H        ;V-RAM adrs low
2120 DATA 62,0:'       MVI    A,00H
2130 DATA 230,191:'    ANI    0BFH       ;write signal = low-level
2140 DATA 211,10:'     OUT    0AH        ;adrs high & write signal set
2150 DATA 219,9:'      IN     09H        ;dummy read
2160 DATA 219,9:'      IN     09H        ;status read
2170 DATA 230,64:'     ANI    40H
2180 DATA 32,250:'     JR     NZ,*-4     ;wait H-SYNC ON
2190 DATA 219,9:'      IN     09H        ;status read
2200 DATA 230,64:'     ANI    40H
2210 DATA 40,250:'     JR     Z,*-4      ;wait H-SYNC OFF
2220 DATA 211,10:'     OUT    0AH        ;write signal reset
2230 DATA 251:'        EI                ;enable interrupt
2240 DATA 201,255:'    RET               ;return
2250 ' *** read routine ***
2510 DATA 243:'        DI                ;disable interrupt
2520 DATA 219,9:'      IN     09H        ;dummy read
2530 DATA 219,9:'      IN     09H        ;status read
2540 DATA 230,64:'     ANI    40H
2550 DATA 32,250:'     JR     NZ,*-4     ;wait H-SYNC ON
2560 DATA 219,9:'      IN     09H        ;status read
2570 DATA 230,64:'     ANI    40H
2580 DATA 40,250:'     JR     Z,*-4      ;wait H-SYNC OFF
2590 DATA 62,0:'       MVI    A,00H
2600 DATA 211,0;'      OUT    00H        ;V-RAM adrs low
2610 DATA 62,0:'       MVI    A,00H
2620 DATA 246,64:'     ORI    40H        ;read signal = high-level
2630 DATA 211,10:'     OUT    0AH        ;adrs high & read signal set
2640 DATA 219,9:'      IN     09H        ;dummy read
2650 DATA 219,9:'      IN     09H        ;status read
2660 DATA 230,64:'     ANI    40H
2670 DATA 32,250:'     JR     NZ,*-4     ;wait H-SYNC ON
2680 DATA 219,9:'      IN     09H        ;read bit-8
2690 DATA 230,128:'    ANI    80H
2700 DATA 50,0,0:'     STA    VRRDA
2710 DATA 219,2:'      IN     02H        ;read data
2720 DATA 50,0,0:'     STA    VRRDB
2730 DATA 251:'        EI                ;enable interrupt
2740 DATA 201,255      RET               ;return
```

資料番号

```
3000 '
3010 ' *** test data parameter ***
3020 DATA 8,8,49,8,7,8,18,49,18,7,8,8,8,18,7,49,8,49,18,7
3030 DATA 10,10,10,16,1,12,10,14,12,1,14,12,12,14,1,17,10,14,16,1
3040 DATA 17,10,20,16,1,24,10,22,12,1,22,12,25,15,1,24,16,22,16,1
3050 DATA 29,10,26,13,1,26,13,29,16,1,29,16,32,13,1,32,13,29,10,1
3060 DATA 29,11,27,13,4,27,13,29,15,4,29,15,31,13,4,31,13,29,11,4
3070 DATA 33,10,33,16,1,35,10,37,12,1,37,12,35,14,1,39,10,39,16,1
3080 DATA 44,10,41,16,1,44,10,47,16,1,-1
3100 DATA 11,10,1,11,14,1,25,10,1,29,12,2
3110 DATA 28,13,2,29,14,2,30,13,2,34,10,1
3120 DATA 34,14,1,-1
```

資料番号

▲ Liquid Crystal Display Control ▲

Bits 2 through 0 of the Color Attribute Byte have the following functions for the Liquid Crystal Display (LCD):

Bit 2 -- For LCD, on which the color attribute is not applied, the character color is assumed as "black". Bit 2 specifies the character color and must be set to "1" (black).

Bit 1 -- This bit is not used.

Bit 0 -- This specifies the following modes:

0: 8-raster mode
8 lines of 40 characters can be displayed on the LCD screen.

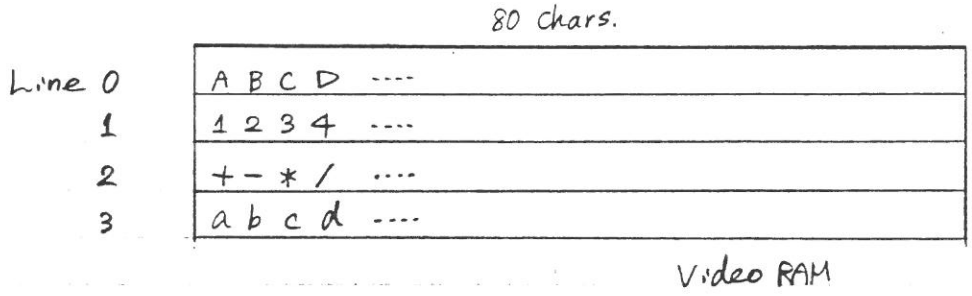
1: 10-raster mode
6 lines of 40 characters can be displayed on the LCD screen.

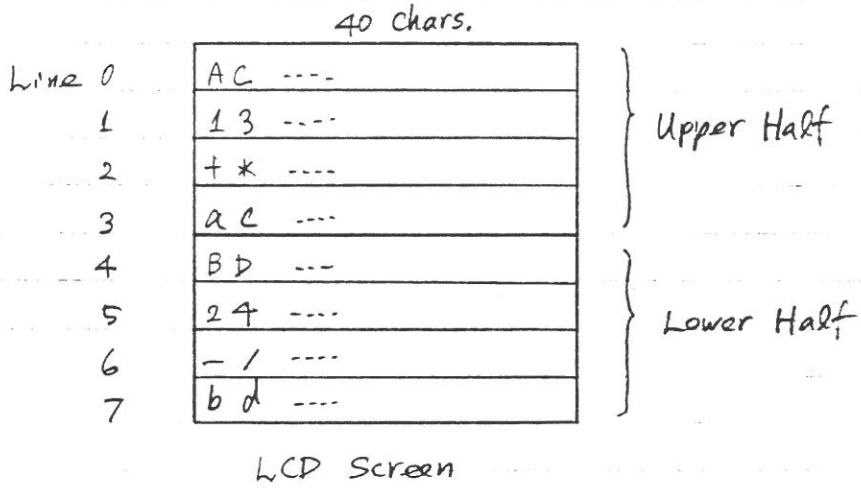
For the background color, the PA0 of the 8255-1 PPI must be set to "0" for 8-raster mode and to "1" for 10-raster mode.
PA2 of the 8255-1 PPI must be set to "0".

Each line is preceded by an Attribute Byte. This is not transferred to the LCD screen.

The LCD screen is divided into upper half and lower half. During one horizontal synch cycle, two lines, one for upper half and the other for lower half, must be transferred from the Video RAM. Consequently, the data structure in the Video RAM and CRT Controller register parameters look differently

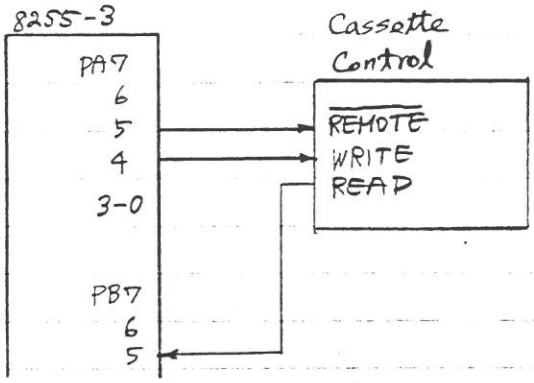
from the screen. The following figures illustrate this for 8-raster mode:





▲ AUDIO CASSETTE INTERFACE ▲

The audio cassette interface is controlled by the 8255 PPI (8255-3).
The cassette output data is written throught output port PA4 of the 8255 PPI. The input data is read by input port PB5. The cassette motor on/off is controlled by output port PA5.



Port	Pin	Active	Function
A (20H)	PA5	L	Cassette motor on/off control
Output	PA4		Cassette write data
B (21H)			
Input	PB5		Cassette read data

A user-supplied cassette recorder can be connected to the 8-pin DIN connector at the rear panel of System Unit. The modulation method used is F-2F. Data is recorded as shown below:

	Byte	Byte	
	Bit	Bit	
	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	

◢ ROM/RAM PACK ◢

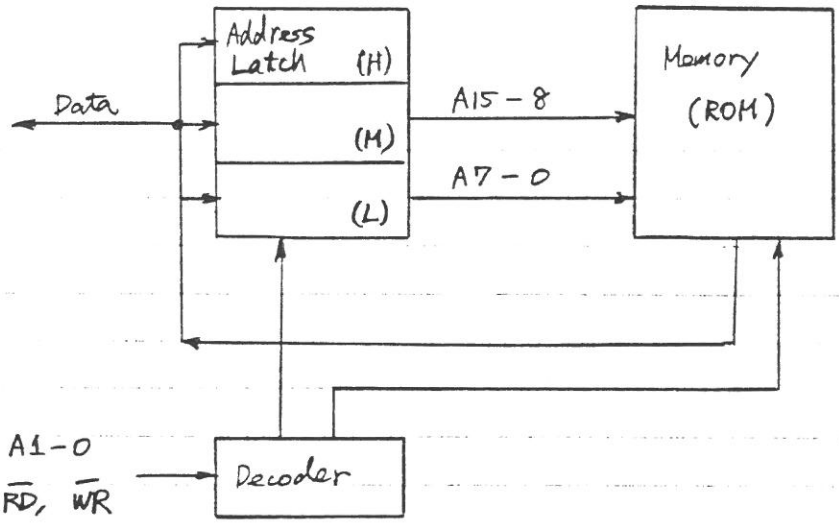
The System Unit has two sockets (Slot 1 and slot 2) to mount external ROM and RAM cartridges (ROM PACK, RAM PACK).

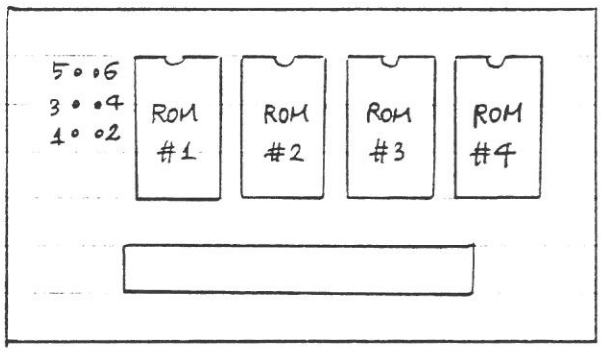
The ROM PACK is plugged in the Slot 1. A ROM PACK can have the storage capacity of up to 32KB. The storage can be accessed by memory bank selection. Refer to Memory Address Space section of this manual.

The RAM PACK or ROM PACK-2 is plugged in the Slot 2. The RAM PACK is composed of static CMOS RAMs which are powered with battery cells. The storage capacity is 16KB (PA7242) or 32KB (PA7244). Data is written to or read from a RAM PACK through the I/O port one byte each time.

There are four ports provided on the system bus. (hex 18, 19, 1A, 1B) The interface logic for these ports are contained in the RAM PACK or ROM PACK2.

A block diagram of ROM PACK and illustration of the jumper connections are on the following page.





Only 64K-bit ROM modules can be used. The storage capacity is selected by the jumper connections as follows:

ROM	Address (Hex)	Jumper
#1	0000 - 1FFF	
#2	2000 - 3FFF	5-6
#3	4000 - 5FFF	3-4
#4	6000 - 7FFF	1-2

Figure ROM PACK

PRINTER INTERFACE

The printer interface is compatible with Centronics parallel interface and controlled by the 8255-3 PPI. Printer data or printer commands are loaded into an 8-bit latched ouput port

A printer interface diagram and table of functions are shown below :

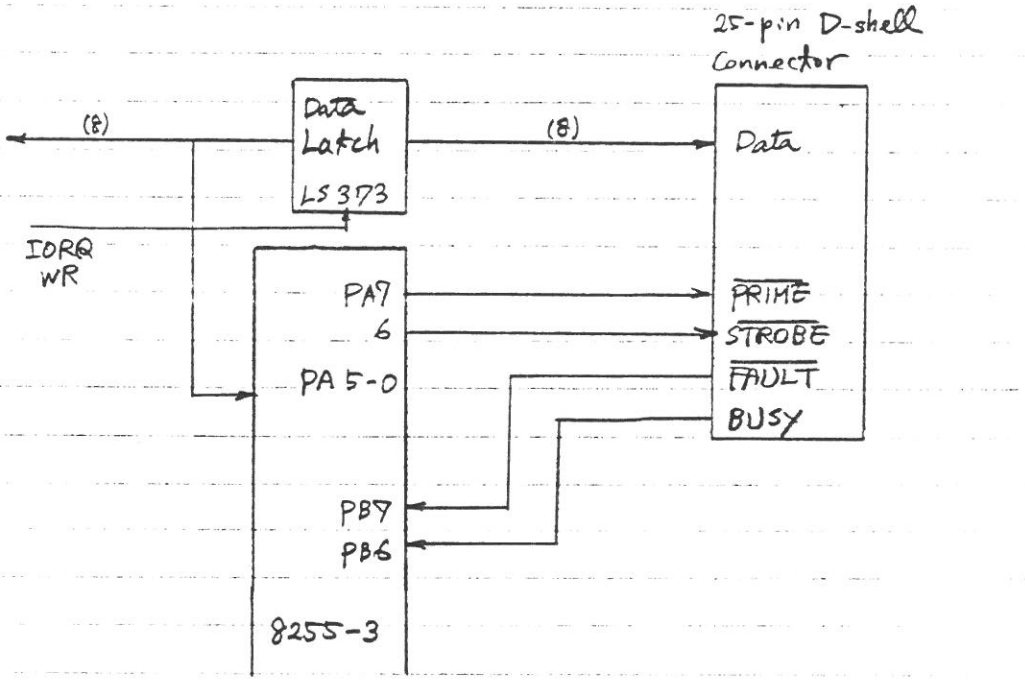


Figure Printer Interface Block Diagram

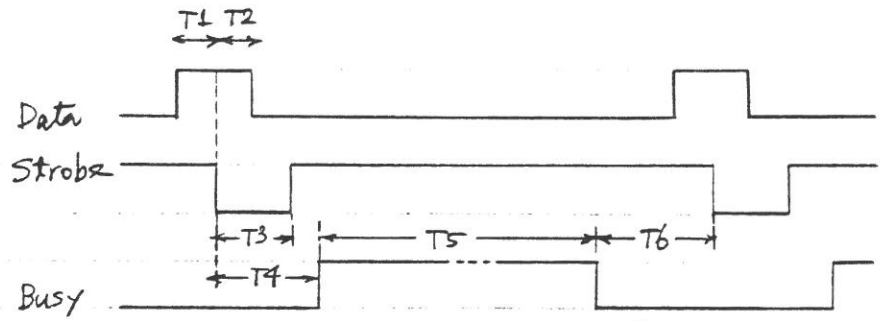
I/O Port	Pin	Active	Description
8255-3 PPI			
A (20H) Output	PA7	H	$\overline{\text{INPUT PRIME}}$: When the level of this signal becomes low, the printer controller is initialized and the print buffer is cleared.
	PA6	H	$\overline{\text{STROBE}}$: This signal is to synchronize read-in of data.
B (21H) Input	PB7	L	$\overline{\text{FAULT}}$: The level of this signal becomes low when the printer is in: • Paper end state • Offline (DESELECT) state • Error state • Cover open
	PB6	H	BUSY : A high signal indicates that the printer cannot receive data.
LS373 (38H)		H	Latched data for printer : 8 bits of parallel data

Note ; High-level signals from PA7 and PA6 of 8255 PPI are inverted to low level to the printer control.

Table Printer Interface Signals

Timing considerations for Dot Matrix Printer (PA7251) and Dot Matrix Printer (PA7252) are as follows:

PA7251



$T1, T2 \geq 0.5\,\mu s$

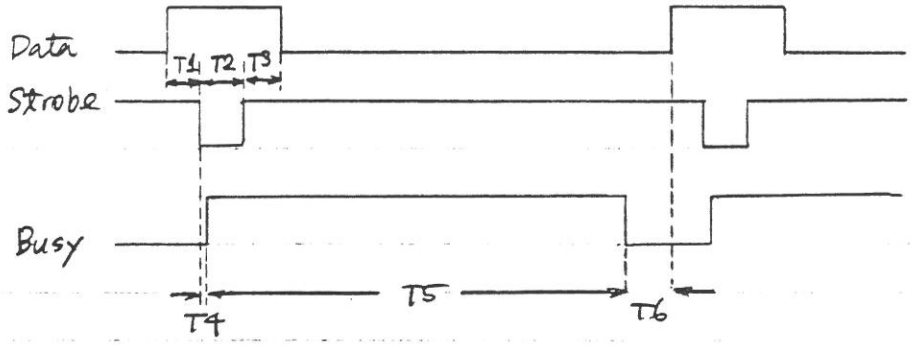
$1\,\mu s \leq T3 \leq 90\,\mu s$: Strobe pulse width

$T4 \geq 30\,\mu s$: It takes minimum 30 μs for the printer control to become busy after strobe signal.

$T5 \geq 60\,\mu s$: Minimum busy duration is 60 μs. Actual duration depends on the input data length.

$T6 \geq 20\,\mu s$: Minimum 20 μs is required before next strobe signal after busy reset.

PA7252



T1, T2, T3 ≥ 1 μs

T4 ≤ 400 ns : It takes maximum 400 ns for the printer to become busy after strobe signal.

100 μs ≤ T5 ≤ 2ms : Normally busy time duration is from 100 μs to 2ms. However when the printer buffer is full, this will be longer.

T6 ≤ 5.5 μs : Maximum 5.5 μs is required before next data signal after busy reset.

▲ 5 1/4" FLOPPY DISK DRIVE UNIT ▲

The 5 1/4" Floppy Disk Drive Unit (PA7200) houses floppy disk controller, two 5 1/4" floppy disk drives, power supply and ventillation fan. The unit is connected to the External Bus Connector of the System Unit.

The floppy disk drive is double-sided, double density with 35 tracks on each side. Each track consists of 16 sectors of 256 bytes. The formatted capacity of a disk is 286,720 bytes.

The floppy disk controller uses the μPD765 controller. The data transfer is performed by IN/OUT instructions without DMA. The interrupt must be prohibited during the data transfer.

A block diagram of floppy disk drive unit is on the following page.

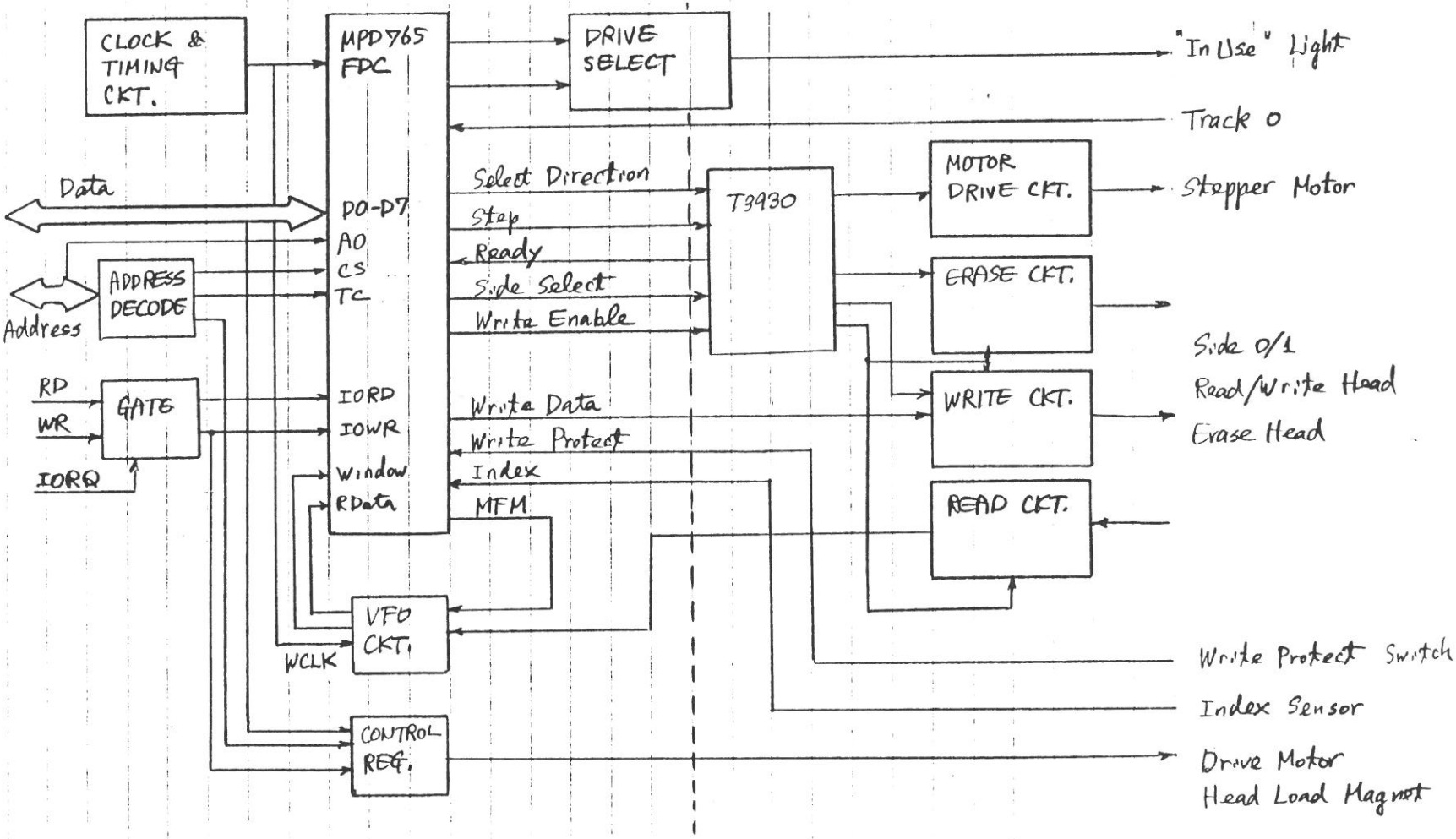


Figure Floppy Disk Drive Unit Block Diagram

Access to the μPD765 Floppy Disk Controller is made through five I/O ports:

Port	Description
E0	FDC TC SIGNAL OFF
E2	FDC TC SIGNAL ON When a byte is written to E0 or E2, the FDC tally count signal is set off or on, respectively. Contents of a byte can be any pattern.
E4	FDC MAIN STATUS REGISTER This contains the status information of the FDC and may be read at any time.

D7	D6	D5	D4	D3	D2	D1	D0
RQM	DIO	NDM	CB	DDB	DCB	DBB	DAB

DAB: FDD number 0 is in the seek mode.
DBB: FDD number 1 is in the seek mode.
CB: A read or write command is in process.
NDM: FDC is in non-DMA mode.
DIO: Indicates direction of data transfer.
1 -- From FDC to CPU
0 -- From CPU to FDC
RQM: Indicates that the FDC Data Register is ready to transfer data.

E5	FDC DATA REGISTER This stores data, commands, parameters and disk drive status.

Port		Description
E6	Bit 7 (D7)	This is used to send the reset signal to the disk drive and to read interrupt request signal from the FDC.
	Bit 6 (D6)	This controls the drive motor on/off : 1 -- Motor on 0 -- Motor off

EXPANSION UNIT

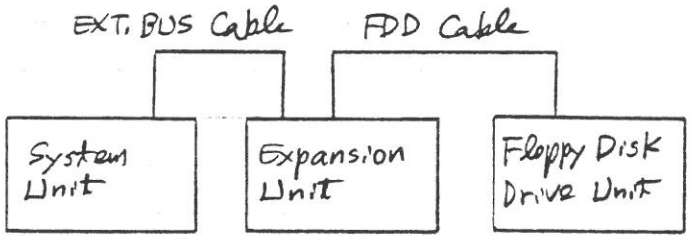
The Expansion Unit (PA7300) is connected to the External Bus Connector of the System Unit and has the following features:

- Expansion Unit Controller
- 5 card edge sockets for option cards
- Floppy Disk Drive Unit interface
- Power Supply

The Expansion Unit Controller has interfaces to the system bus of the System Unit CPU board, option cards and Floppy Disk Drive Unit.

Up to five option cards can be plugged vertically in the card edge sockets of the Expansion Unit Controller. The power +5V, +12V and -12V are supplied through these sockets to the option cards. Examples of option cards are RS-232C and GPIB interface cards.

When both Expansion Unit and Floppy Disk Drive Unit (PA7200) are configured in a system, they are connected as follows:



The Expansion Unit Controller accepts the interrupt requests from the option cards and transmits the requests to the System Unit with the interrupt vector "FF (hex)". The program identifies the interrupt source by reading the contents of Interrupt Request Level Register and Read ID Registers.

A block diagram of Expansion Unit Controller is shown below :

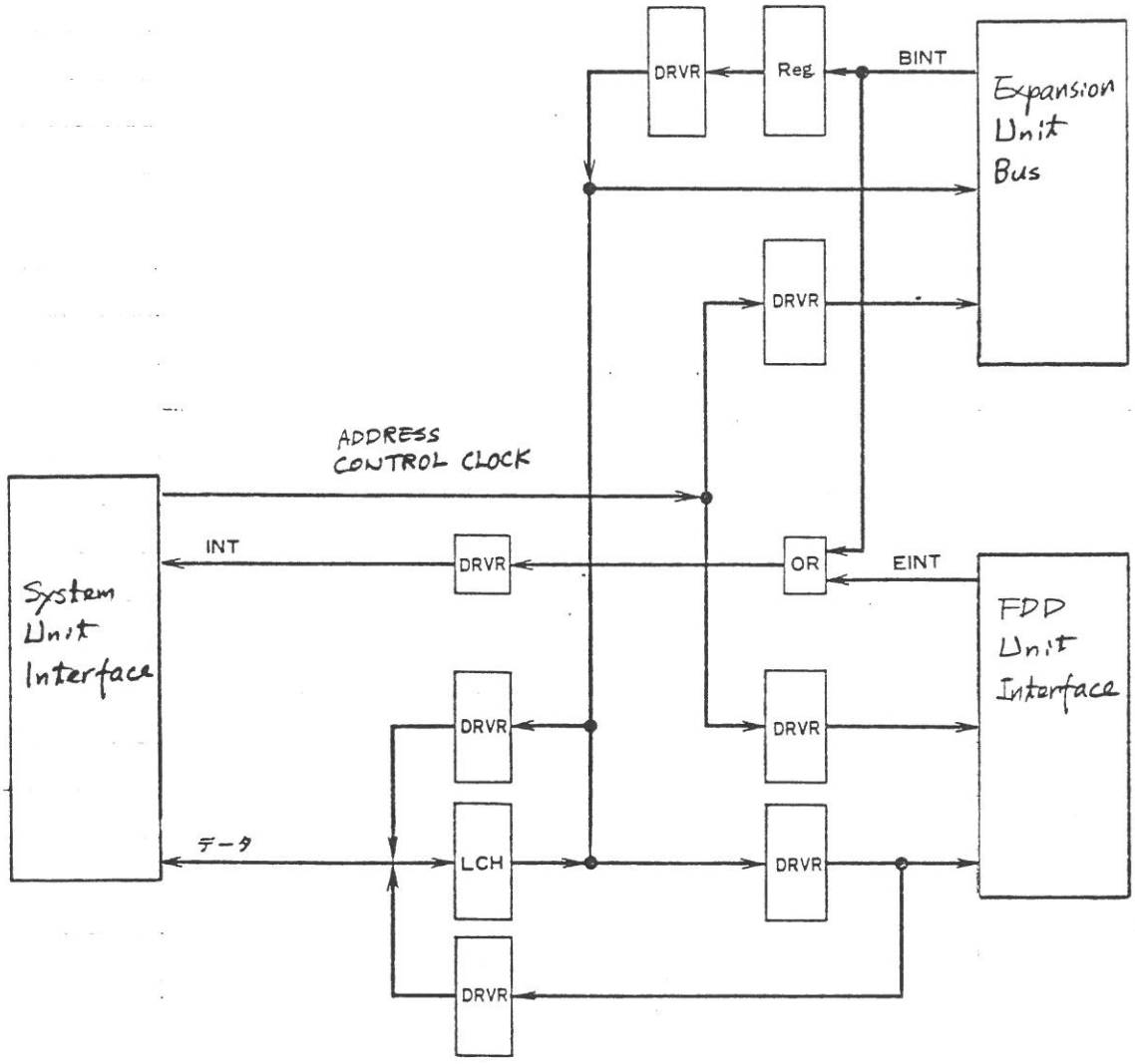


Figure Expansion Unit Controller Diagram

Interrupt Request Level Register

I/O Port	I/O	Data Bits							
4F	Read	Bit 7	6	5	4	3	2	1	0
		1	1	$\overline{L5}$	1	$\overline{L3}$	$\overline{L2}$	$\overline{L1}$	$\overline{L0}$

This register is on the Expansion Unit Controller and indicates the level of interrupt request from an option card.
Interrupt request levels are defined by the hardware. Levels L0 through L3 are assigned uniquely to option cards. Level L5 is assigned to more than one option cards.

Option Card	Level
RS232C Interface	L1
GPIB Interface	L5

I/O Select Register - 1

I/O Port	I/O	Data Bits							
DF	Write	Bit 7	6	5	4	3	2	1	0
		Read	I/O	I/O	I/O	I/O	I/O	I/O	I/O
		SEL-1	6	5	4	3	2	1	0

This register is provided on the option cards which have the interrupt request level L5. The I/O port addresses D0 through DD (hex) are assigned to Control Registers on the option cards with level L5. By setting one of the bits I/O 6 through I/O 0, ports D0 through DD are allocated to the corresponding option.

By resetting the bit, ports D0 through DD are deallocated from the option.

Option Card	Bit
GPIB Interface	I/O 0

Bit 7 (Read SEL-1) defines the read mode for Read ID Register-1.

Read ID Register-1

I/O Port	I/O	Data Bits							
		7	6	5	4	3	2	1	0
DF	Read	1	$\overline{ID6}$	$\overline{ID5}$	$\overline{ID4}$	$\overline{ID3}$	$\overline{ID2}$	$\overline{ID1}$	$\overline{ID0}$

This register is provided on the option cards which have the interrupt request level L5.

When Read SEL-1 (I/O Select Register-1) is 0, the data bits indicate the selected option to which ports D0 through DD have been allocated.

When Read SEL-1 is 1, the data bits indicate the options which have outstanding interrupt requests of level L5.

Option Card	Bit
GPIB Interface	IDO

I/O Select Register - 2

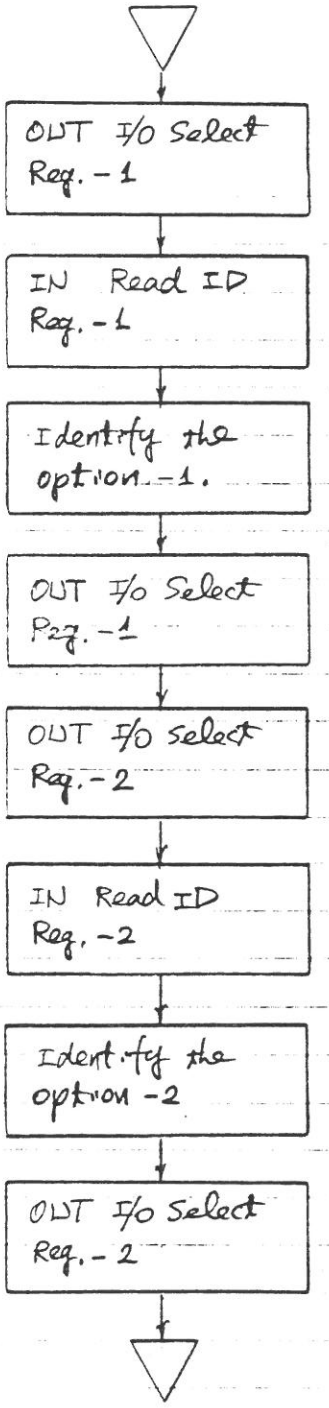
I/O Port	I/O	Data Bits							
DE	Write	Bit	7	6	5	4	3	2	1	0
		Read SEL-2	I/O D	I/O C	I/O B	I/O A	I/O 9	I/O 8	I/O 7

Read ID Register - 2

I/O Port	I/O	Data Bits							
DE	Read	Bit	7	6	5	4	3	2	1	0
			1	$\overline{IDD}$	$\overline{IDC}$	$\overline{IDB}$	$\overline{IDA}$	$\overline{ID9}$	$\overline{ID8}$	$\overline{ID7}$

These are assigned to the additional options with the interrupt request level L5 and work similarly as I/O Select Register - 1 and Read ID Register - 1.

Examples of programs to identify the options configured, to access an option and to process the interrupt requests are on the following pages.



(NOTES)

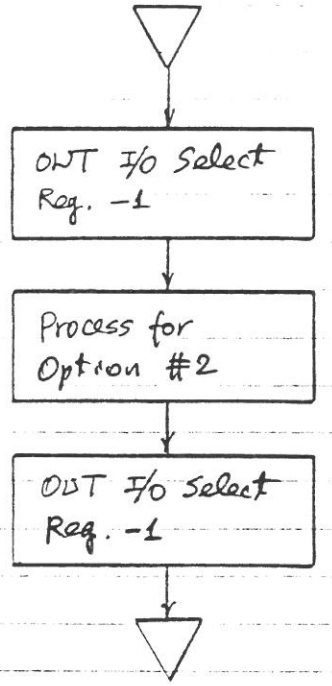
Write (7F)H to select.

Write (00)H to deselect.

Write (7F)H to select.

Write (00)H to deselect.

Figure Option Card Identification



(NOTES)

Write (04)H to select option #2.

Write (00)H to deselect option #2.

Figure Process for Option Card #2

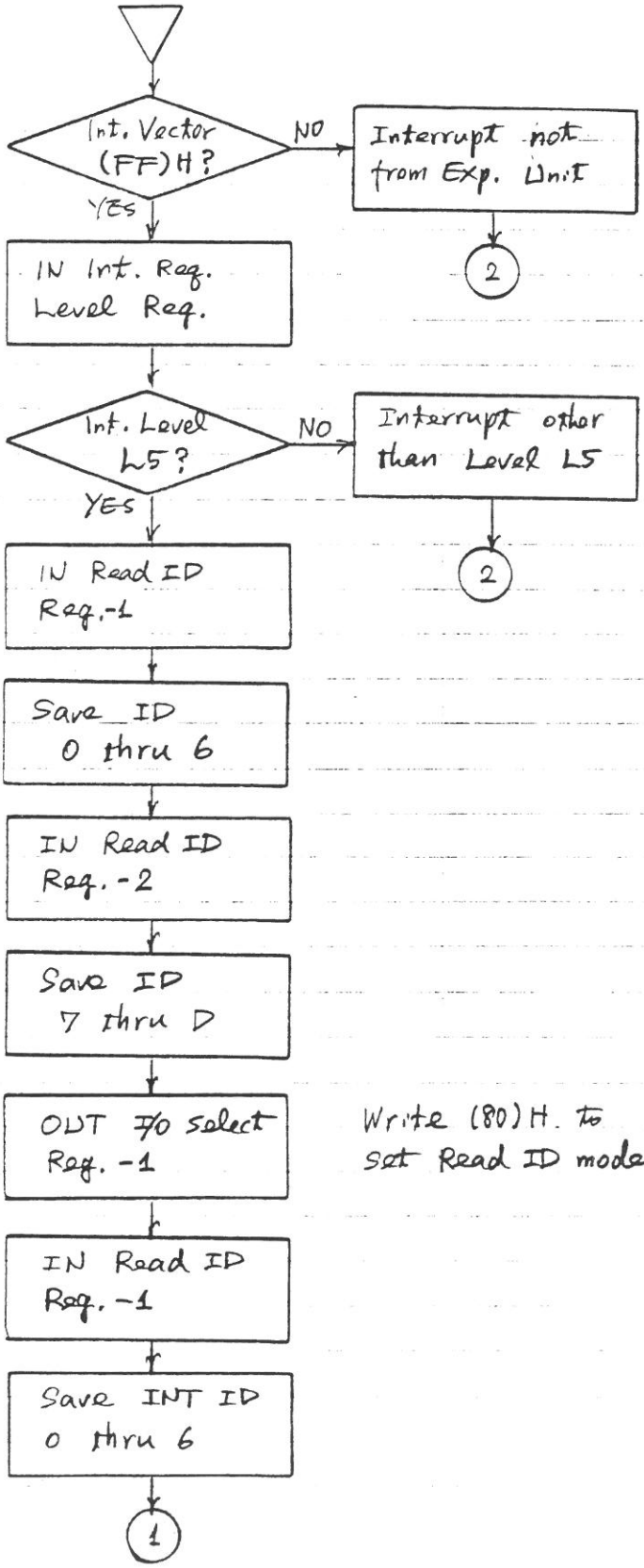


Figure Interrupt Processing

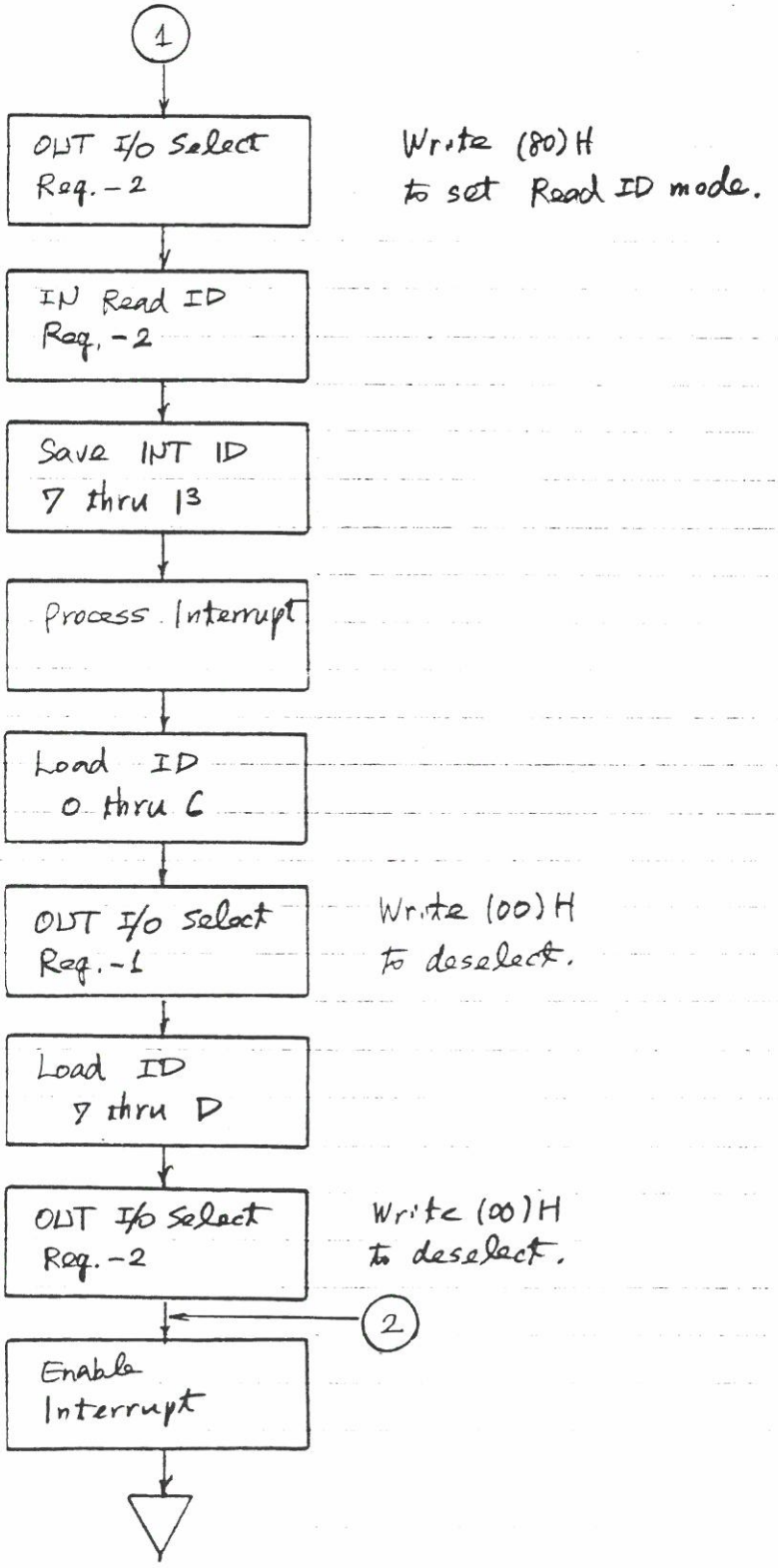


Figure Interrupt Processing (continued)

The Expansion Unit Controller has five 72-pin card edge sockets for option cards. Descriptions of signal lines are on the following pages.

The following symbols are used in these descriptions :

DIRECTION : Signal direction
C -- Expansion Unit Controller
O -- Option Card

+5V -- DC +5V
+12V -- DC +12V
-12V -- DC -12V
GND -- Ground DC 0V

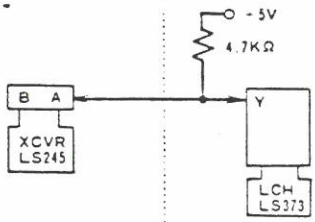
SIGNAL :

ABCDEF : OOO
- OOO: Signal Polarity
- ABCDEF: Signal Name

PIN	SIGNAL	DIRECTION C	DIRECTION O	PIN	SIGNAL	DIRECTION C	DIRECTION O
B01	+5V			A01	+5V		
B02				A02			
B03				A03			
B04				A04			
B05				A05	GND		
B06				A06			
B07				A07			
B08				A08	BCAD07 : 000		→
B09	BCAD06 : 000	→		A09	GND		
B10	BCAD05 : 000	→		A10	BCAD04 : 000	→	
B11	BCAD03 : 000	→		A11	BCAD02 : 000	→	
B12	BCAD01 : 000	→		A12	BCAD00 : 000	→	
B13	BCZDB7 : 100	↔		A13	GND		
B14	BCZDB6 : 100	↔		A14	BCZDB5 : 100	↔	
B15	BCZDB4 : 100	↔		A15	BCZDB3 : 100	↔	
B16	BCZDB2 : 100	↔		A16	BCZDB1 : 100	↔	
B17	+12V			A17			
B18	GND			A18	BCZDB0 : 100	↔	
B19	BINT5 : 000	←		A19	BINT3 : 000	←	
B20	−12V			A20			
B21	BINT2 : 000	←		A21	GND		
B22	BINT1 : 000	←		A22	BINT0 : 000	←	
B23				A23			
B24				A24			
B25				A25	GND		
B26				A26			
B27				A27	BCRST : 000	→	
B28				A28			
B29				A29	GND		
B30				A30			
B31				A31			
B32				A32	BCRD : 000	→	
B33	BCWR : 000	→		A33	GND		
B34	BS8MHZ : 000	→		A34			
B35				A35			
B36	+5V			A36	+5V		

Table Expansion Slot Signals (1)

PIN	SIGNAL	DESCRIPTION	CIRCUIT	
			OPTION	EXP. UNIT CONT.
A08	BCAD07 :000	Address Lines: 2^7		
B09	BCAD06 :000	2^6		
B10	BCAD05 :000	2^5		
A10	BCAD04 :000	2^4		
B11	BCAD03 :000	2^3		
A11	BCAD02 :000	2^2		
B12	BCAD01 :000	2^1		
A12	BCAD00 :000	2^0		
B13	BCZDB7 :100	Data Lines: 2^7		
B14	BCZDB6 :100	2^6		
A14	BCZDB5 :100	2^5		
B15	BCZDB4 :100	2^4		
A15	BCZDB3 :100	2^3		
B16	BCZDB2 :100	2^2		
A16	BCZDB1 :100	2^1		
A18	BCZDB0 :100	2^0		
A32	BCRD :000	Read request from the register specified by the address lines.		
B33	BCWR :000	Write request to the register specified by the address lines.		
B34	B$8MHZ:000	7.9872 MHz Clock		



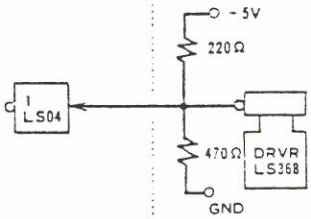


Table Expansion Slot Signals (2)

PIN	SIGNAL	DESCRIPTION	CIRCUIT	
			OPTION	EXP. UNIT. CONT.
B19	BINT5 :000	Interrupt Req. Level : L5		
A19	BINT3 :000	L3		
B21	BINT2 :000	L2		
B22	BINT1 :000	L1		
A22	BINT0 :000	L0		
A27	BCRST :000	Reset signal generated at : Exp. Unit Power on System Unit Power on System Reset		

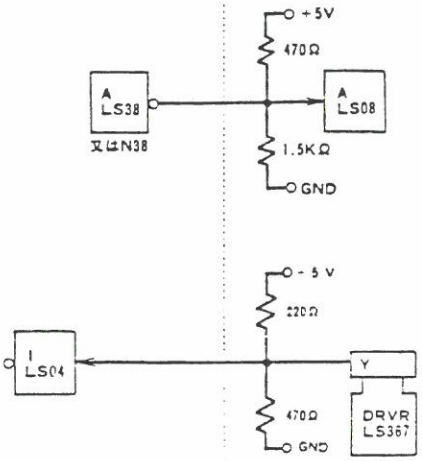


Table Expansion Slot Signals (2) (continued)

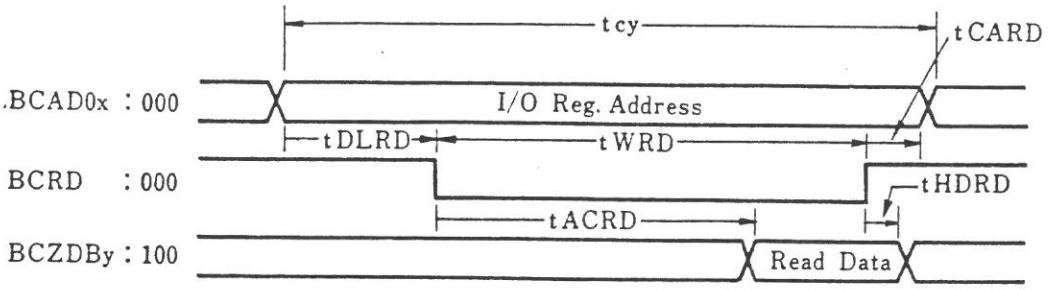


Figure Timing for Data Read

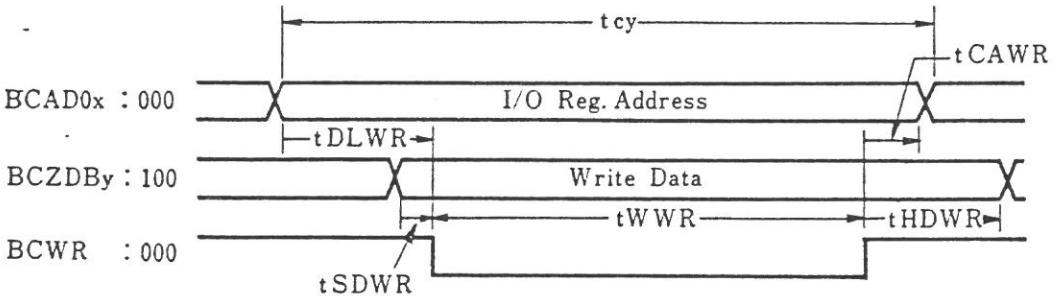


Figure Timing for Data Write

SIGNAL	MIN(ns)	TYP(ns)	MAX(ns)
tcy		1000	
tDLRD	85	—	—
tWRD	440	—	730
tACRD	—	—	310
tHDRD	0	—	100
tCARD	20	—	—
tDLWR	85	—	—
tSDWR	−280	—	150
tWWR	440	—	730
tHDWR	100	—	—
tCAWR	20	—	—

Table AC Characteristics

▲ RS-232C INTERFACE ▲

An integrated RS-232C communication port is provided on the CPU Board of the System Unit with a 25-pin D-type connector at the back of the System Unit. This is capable of communicating in up to 600 bps.

In addition to this, one or two optional RS-232C ports are brought to the system by option cards that are plugged in the Expansion Unit. These can communicate in up to 9600 bps.

Summarized functions of these RS-232C ports are as shown below:

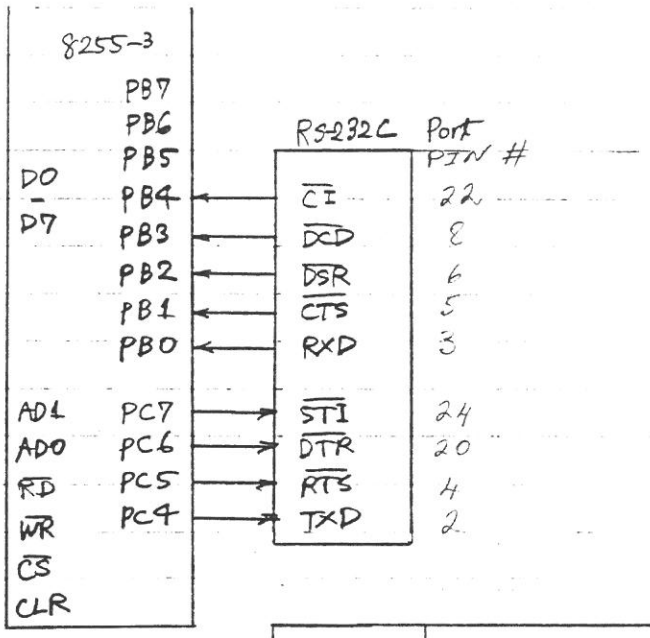
	Integrated Port	Optional Port
No. of Lines	1	1
Line	Leased or Switched	Leased or Switched
Comms. Method	Asynch Half-duplex	Asynch, Synch Half-duplex
Transmission Rate (bps)	75, 110, 150 300, 600	75~600, 1200, 2400, 4800, 9600
Character Code	5, 6, 7, 8 bit	5, 6, 7, 8 bit
Parity Check	Odd, Even, None	Odd, Even, None
No. of Stop Bits	0, 1, 1.5, 2	1, 1.5, 2

Table RS-232C Ports

Details of T-BASIC statements used for communications are explained in the T-BASIC section of this manual.

▲ Integrated RS-232C Port ▲

The integrated RS-232C interface is composed of channels B and C of the 8255 PPI (8255-3). All transmission controls are performed by the software. A block diagram of this interface is as shown below:



Signal	Description
CI	Carrier Detect
DCD	Received Line Signal Detector
DSR	Data Set Ready
CTS	Clear to Send
RXD	Receive Data
STI	Trans. Signal Element Timing
DTR	Data Terminal Ready
RTS	Request to Send
TXD	Transmit Data

Figure Integrated RS-232C Port

Expansion Unit RS-232C Card

One or two RS-232C option cards can be plugged in the expansion slots of the Expansion Unit to bring the system one or two programmable RS-232C ports.

Each card contains i8251A compatible USART, i8253-5 PIT, additional registers and 25-pin D-type connector. A DIP switch is also provided on each card and is set as follows:

SW-1 -- OFF
SW-2 -- OFF for first RS-232C card
ON for second RS-232C card
SW-3 -- ON to enable transmit interrupt
OFF to disable transmit interrupt
SW-4 -- OFF

NOTE: SW-3 is set OFF for T-BASIC programs.

A block diagram of RS-232C card is shown below:

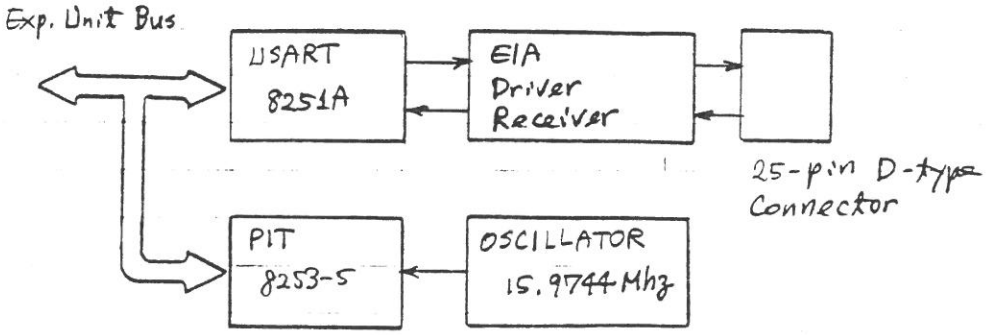
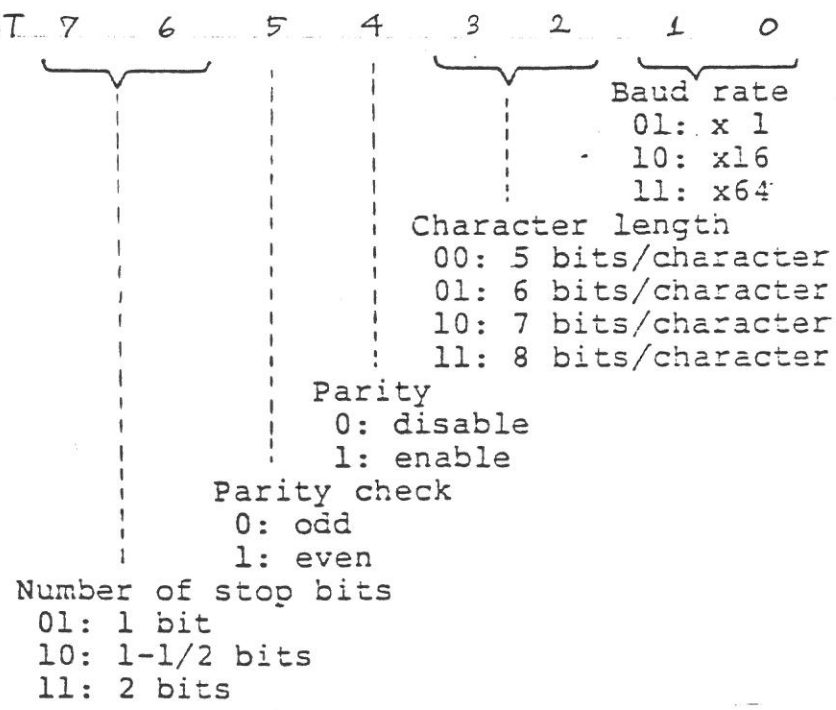


Figure Expansion Unit RS-232C Interface

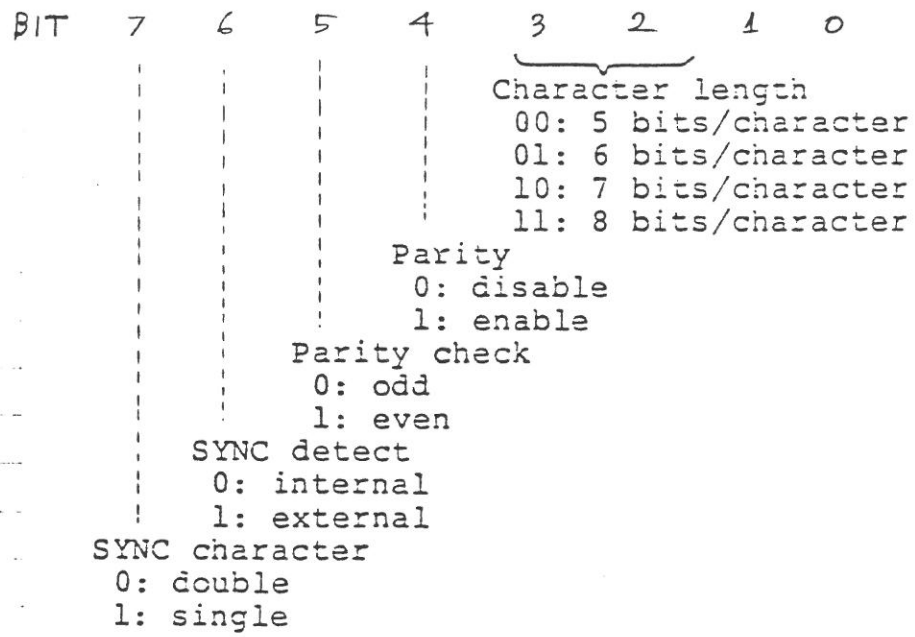
The I/O ports are assigned as follows:

Port	I/O	Register
D0	R/W	8253 Counter #0
D1	R/W	8253 Counter #1
D2	R/W	8253 Counter #2
D3	W	8253 Counter Control
D4	R/W	8251 Data
D5	R/W	8251 Control/Status
D6	R/W	CCM Mode Register
D7	R	CI/CTS Status Register

8251A Mode Instruction (Asynchronous)



8251A Mode Instruction (Synchronous)



8251A Command Instruction

BIT	7	6	5	4	3	2	1	0
	EH	IR	RTS	ER	SBRK	RXE	DTR	TXEN

EH Enter Hunt mode
1: Searching for SYNC character

IR Internal Reset
1: initial setting

RTS Request To Send
1: $\overline{RTS} = 0$

ER Error Reset
1: reset the error flag (PE, OE, FE)

SBRK Send Break
1: TXD = LOW

RXE Receive Enable
1: enable
0: disable

DTR Data Terminal Ready
1: $\overline{DTR} = 0$

TXEN Transmit Enable
1: enable
0: disable

8251A Status

DSR	SYN DET	FE	OE	PE	TXE	RX RDY	TX RDY

DSR	Data Set Ready
SYNDET	SYNC Character Detected
FE	Framing Error (ASYNC only)
OE	Overrun Error
PE	Parity Error
TXE	Transmitter Empty
RXRDY	Receiver Ready
TXRDY	Transmitter Ready

8253-5 PIT

In asynchronous mode, only Counter #2 is used. Mode 3 and binary count must be specified. Transmission rates are set as follows:

Baud Rate	Contents Written (Decimal)
110	1135
150	832
300	416
600	208
1200	104
2400	52
4800	26

In the case of synchronous mode with clock supplied from the modem, 8253-5 PIT need not be programmed.

In synchronous mode and when the internal clock is used, PIT must be set as follows:

Counter #0	Mode 1, binary count
Counter #1	Mode 1, binary count
Counter #2	Mode 2, binary count

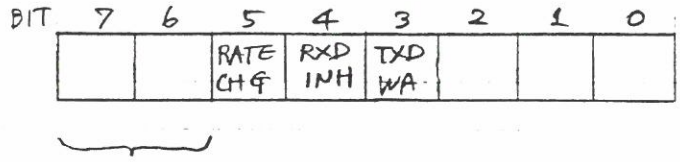
	Contents Written (Decimal)		
Baud Rate	Counter #0	Counter #1	Counter #2
1200	624	728	104
2400	312	364	52
4800	156	182	26
9600	78	91	13

The clock input to PIT is 1.9968 Mhz.

Counter #0 : 1.9968 Mhz × 1/N × 3/8
Counter #1 : 1.9968 Mhz × 1/N × 7/16
Counter #2 : 1.9968 Mhz × 1/N × 16
where N is the transmission rate.

CCM Mode Register

This register is used to set the clock source or to clear the receive buffer.

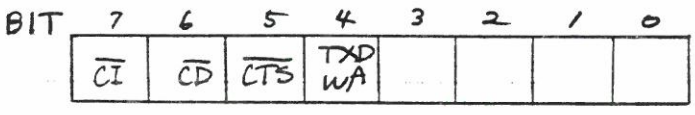


00 -- Acynchronous
01 -- Synchronous (modem clock)
10 -- Synchronous (internal clock)
11 -- Synchronous (direct connection)

RATE CHG : Change Modem Speed
0 -- Normal
1 -- Half
RXDINH : Inhibits RXD input.
TXDWA : Sends back internally the transmitted data.

CI/CTS Status Register

This register provides the additional status information of the interface.



CI : Call Indicator
CD : Carrier Detect
CTS : Clear to Send
TXDWA : Reflects TXDWA bit of CCM Mode Register.